Reed Electronics Group

# EDN

VOICE OF THE ENGINEER

FEB 21

Issue 4/2008

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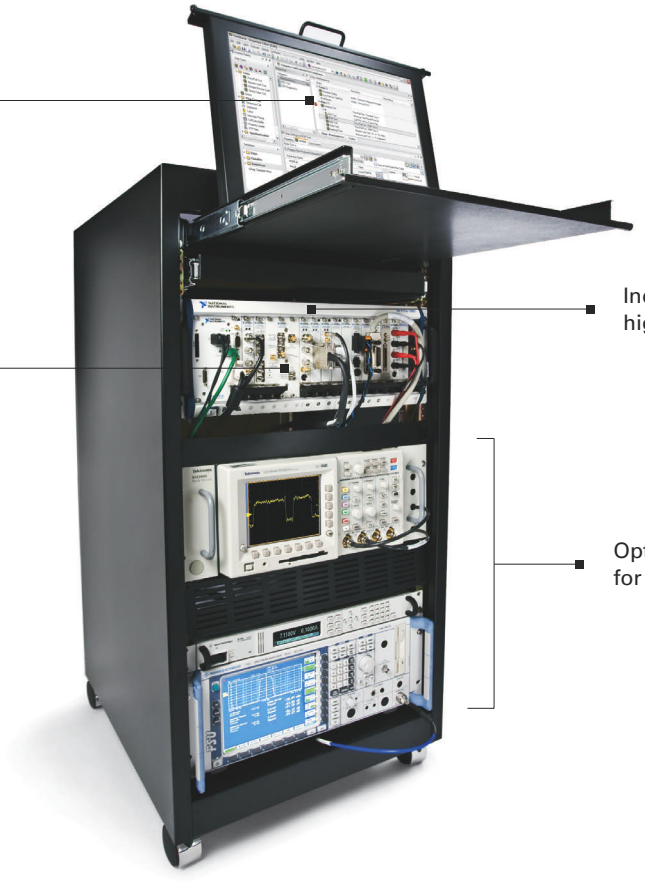

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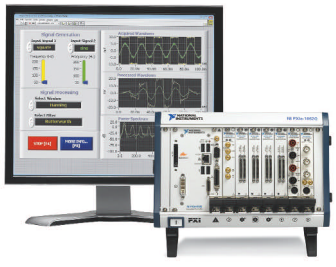

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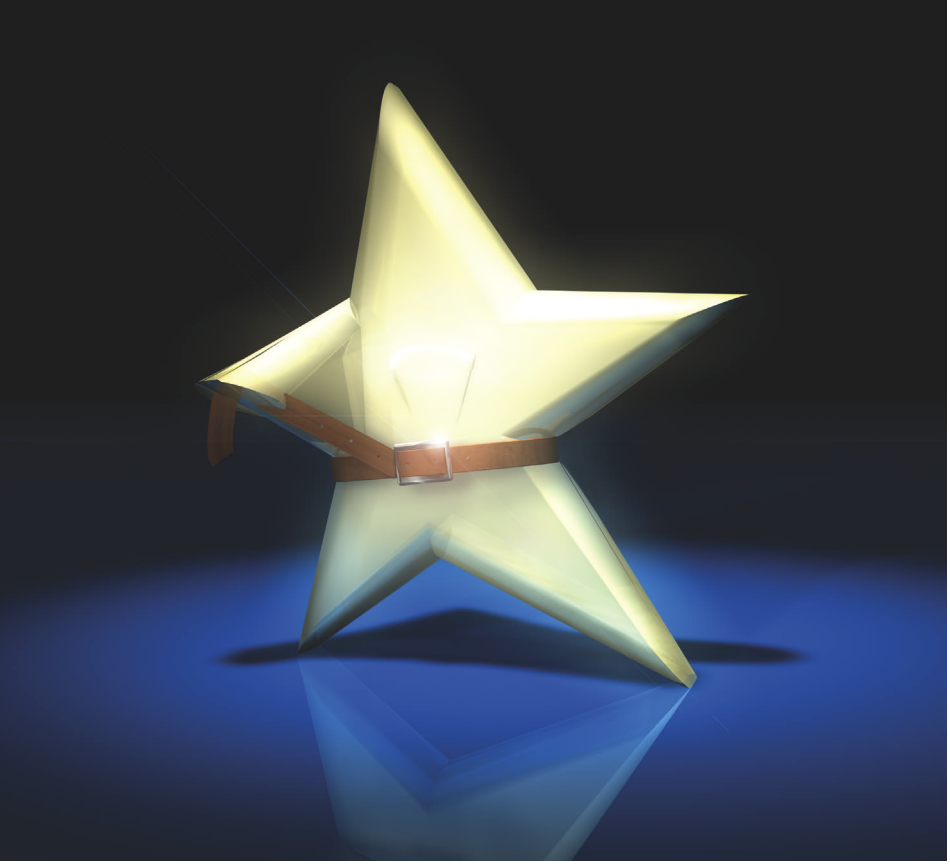

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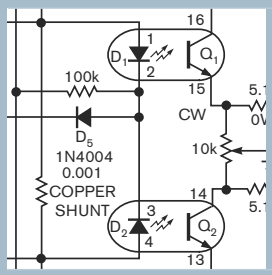


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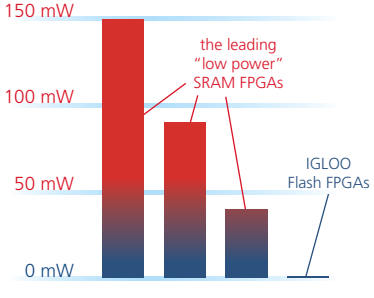


At 148 µW, IGLOO static power use is barely visible compared to equivalent gate parts from the nearest competitors, which use from 300 to 1500 times more power.

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POWER MATTERS

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## pulse

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## DEPARTMENTS & COLUMNS



## PRODUCT ROUNDUP




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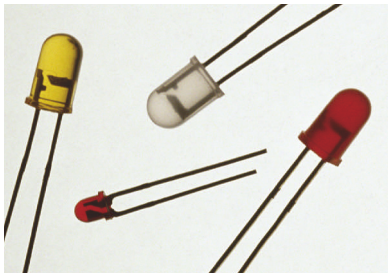

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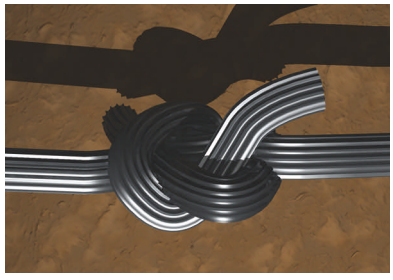

## READERS' CHOICE

*A selection of recent articles receiving high traffic on www.edn.com.*

**Overengineering: How much is too much?**
My father's WWII tale about Allied versus German telephones contained a valuable design lesson.
→www.edn.com/article/CA6518684

**EEs have terrorist mindset, Oxford University paper suggests**
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**A solar panel on every building**
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**If Apple won't buy AMD, how about IBM?**
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**System (un)reliability: The Microsoft Xbox 360 case study**
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**Intel moves last Silicon Valley fab from manufacturing to process development**
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## WE NEED YOUR VOTE!

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## FROM *EDN*'s BLOGS

**Should power management be application-specific?**

*From Practical Chip Design, by Ron Wilson*
Most power-management approaches focus on maximum flexibility to turn blocks on and off quickly, because little is known about the application and its use models at design time. But if you know the application in detail, you can tailor a power-management strategy to it from the ground up.
→www.edn.com/080221toc4

BY MAURY WRIGHT, EDITORIAL DIRECTOR

# *EDN* Innovation: Awards season comes to technology

In the Feb 7 issue of *EDN*, we announced the finalists for the 18th edition of our *EDN* Innovation Awards program. We strive to recognize the brightest technologies and engineers each year, and this year we have a ballot full of innovation. Every year, the Innovation Awards coincide with some well-known awards in the entertainment industry. We consider ours far more important. This year, our voting process will also coincide with national presidential primaries. I certainly hope that all eligible voters turn out for both the Innovation and the presidential contest. To be eligible to vote in Innovation, we ask only that you wade through tough ballot choices, carefully consider the outstanding finalists, and make your selection.

Engineers rarely receive the same fame as those that toil in some higher profile professions. But I don't know of a job that demands a better combination of technical savvy, theoretical knowledge, and creative thought process than electronics engineering. Our 2007 salary and career survey indicated that those aspects of the job are more important to working engineers than the financial rewards.

Everyone needs a nice "attaboy" now and then. We think the winners that emerge from our multistage Innovation selection process deserve a fancy banquet and party. If our program includes your work, congratulations and good luck.

You will find a list of the finalists and voting information at www.edn.com/innovation. This year, we have 19 product/technology categories plus the *EDN* Innovator of the Year, which recognizes an engineer or engineering team. We also include a category for the best article contributed to *EDN* in 2007.

The number of Innovation categories is at an all-time high. The expanded roster is due in part to the popularity of the program and the sheer number of entries. Frankly, the trend of specialization in everything from analog ICs to test equipment demanded the expansion. With so many application-specific products, our editors and judges have an increasingly difficult time making apples-to-apples comparisons. I think you will agree as you peruse the list that there is just more innovation today than ever before. Moore's Law advancements have brought unprecedented processing power, the transition to digital media, and a vast array of applications. Meanwhile, analog technology has kept up and provides the quality user experience as the interface to the real world.

**With so many application-specific products, our editors and judges have an increasingly difficult time making apples-to-apples comparisons.**


When you view the finalists list, you will find short descriptions of the innovation in each of the entries. In the case of Innovator of the Year, you will also learn a little of the biographical background of the entry. And, in the case of the best contributed article, you will get a pointer to the article. Please take the time to participate in our program. The finalists deserve your consideration, and you may one day find your own work or yourself on the list.

I also encourage anyone who can be in San Jose, CA, on April 14 to consider attending the banquet. Tickets cost $110, and you can buy them at the www.edn.com/innovation Web link. The fee covers a cocktail party, a nice dinner, some outstanding entertainment, a chance to recognize your peers, and entrée to an Oscar-worthy afterparty. See you in San Jose and happy voting. EDN

*Contact me at mgwright@edn.com.*

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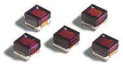
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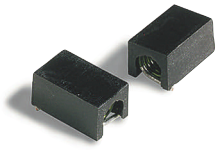
Maxi Spring Air Coils

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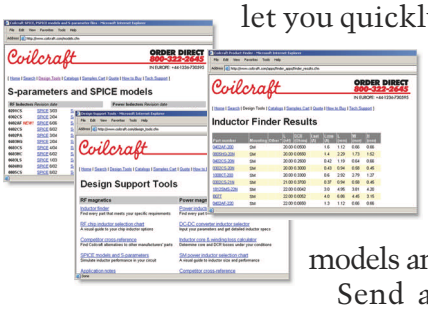


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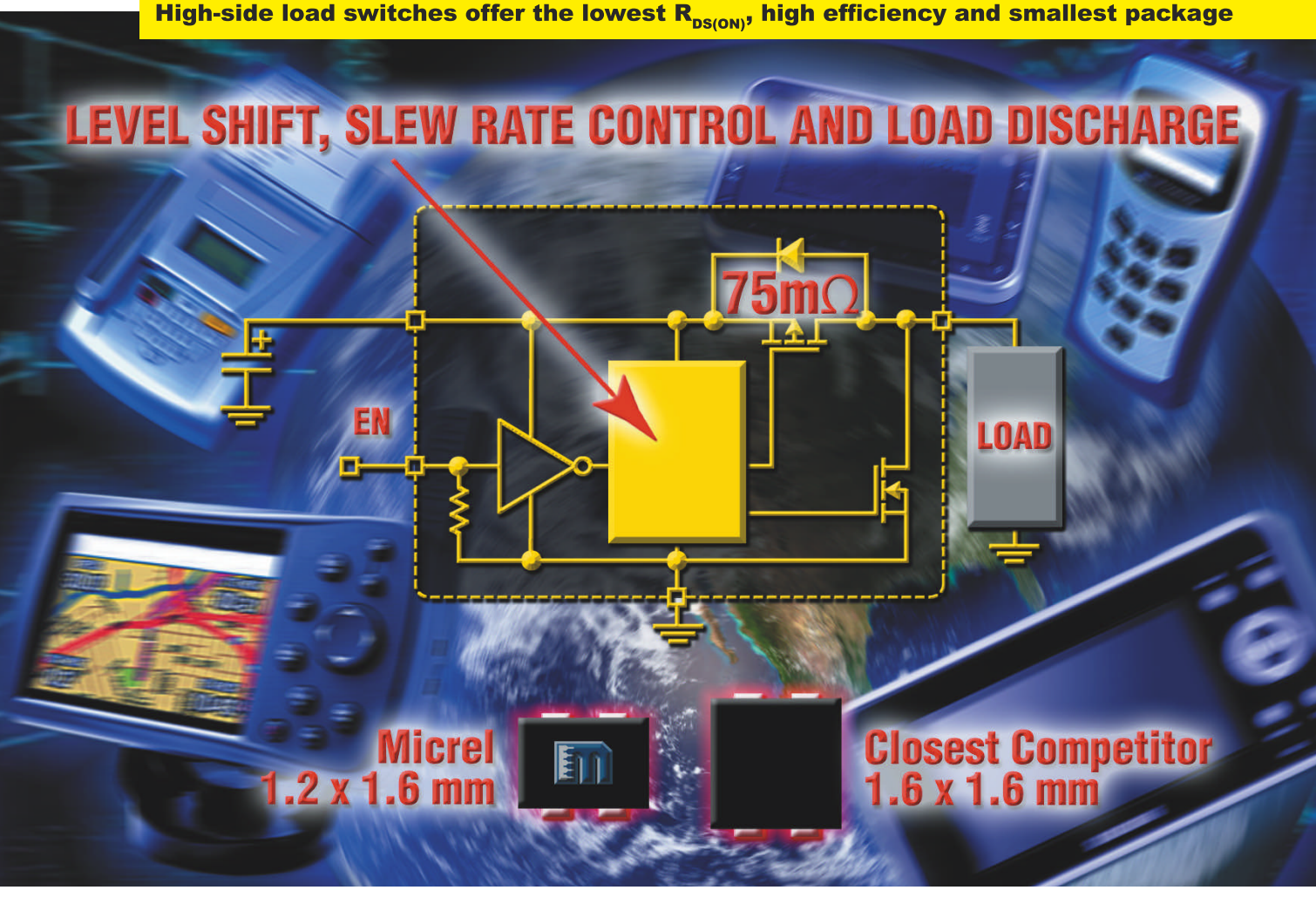


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- Active Load Discharge at Shutdown

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Literature 1 (408) 435-2452 Information 1 (408) 944-0800



| | MIC94060 | MIC94061 | MIC94062 | MIC94063 |
|---|---|---|---|---|
| $V_{IN}$ | 1.7V to 5.5V | 1.7V to 5.5V | 1.7V to 5.5V | 1.7V to 5.5V |
| $R_{DS(ON)}$ - SC70 | 75mΩ | 75mΩ | 75mΩ | 75mΩ |
| $R_{DS(ON)}$ - MLF | 85mΩ | 85mΩ | 85mΩ | 85mΩ |
| $I_{MAX}$ | 2A | 2A | 2A | 2A |
| $I_{SHUT-SUPPLY}$ | 2nA | 2nA | 2nA | 2nA |
| $I_{SHUT-LEAKAGE}$ | 2nA | 2nA | 2nA | 2nA |
| $t_{ON-DLY}$ | 0.85µs | 0.85µs | 700µs | 700µs |
| $t_{ON-RISE}$ | 1µs | 1µs | 800µs | 800µs |
| $t_{OFF-DLY}$ | 100ns | 100ns | 60ns | 60ns |
| $t_{OFF-FALL}$ | 60ns | 60ns | 60ns | 60ns |
| Package | 1.2x1.6 MLF®-4 SC-70-6 | 1.2x1.6 MLF®-4 SC-70-6 | 1.2x1.6 MLF®-4 SC-70-6 | 1.2x1.6 MLF®-4 SC-70-6 |
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RENESAS M16C Platform

# M16C - Protecting code investment with true code & pin compatibility

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### No.1* supplier of microcontrollers in the world

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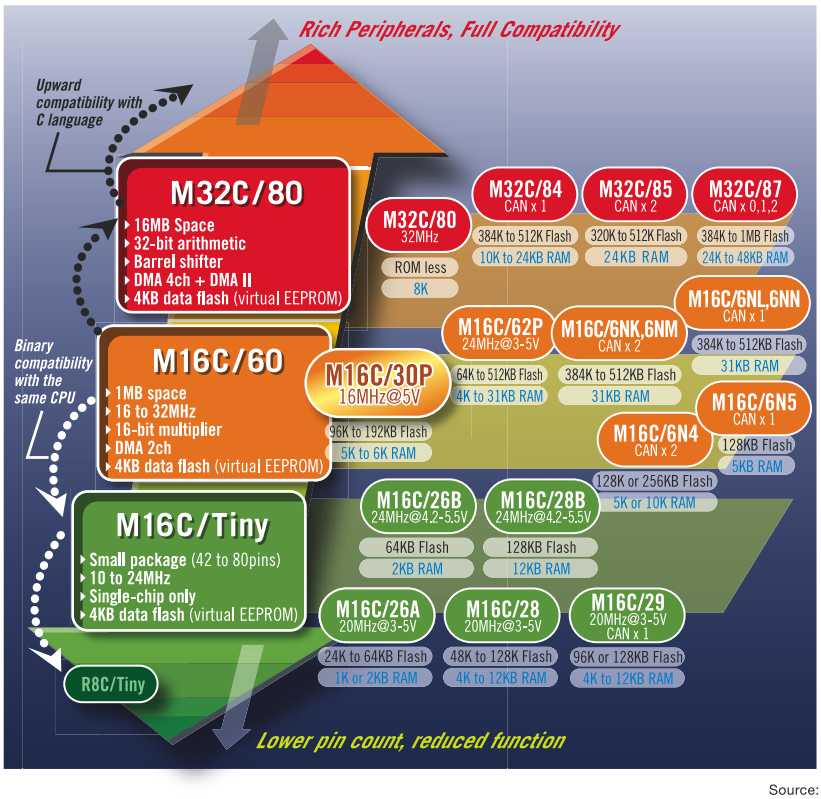
**M16C Product Lineup**

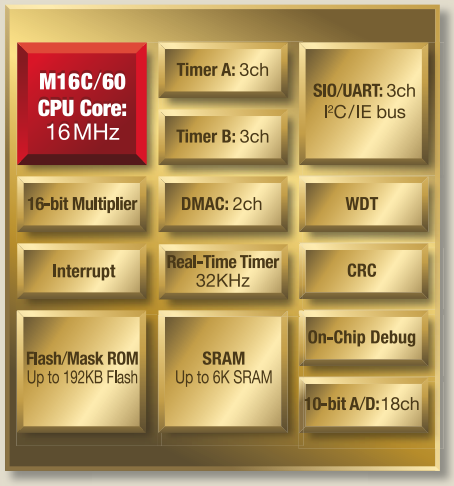



**HOT Products** | **M16C/30P Group**

3 cents per pin*

* M30302FCPGP#U5C 100 pin LQFP 128K Flash /5K RAM

**M16C/30P Block Diagram**




### Top Reasons to select M16C MCU

- **Broad Platform & Compatibility**
  - Wide selection; 24KB to 1MB Flash, 42 to 144 pin
  - Up/downgrade in same package, same board design
  - Saves costs and protecting code investment.
- **Powerful and Easy**
  - Banked registers & high speed interrupts (M32C)
  - Optimized instructions for 1cycle operations
  - High-speed hardware multiplier
  - Common Tool Chain across the platform
  - Proven middleware; ZigBee, CAN, motor control
- **Versatile & Efficient**
  - Specialized peripherals; CAN, PLC, motor control
  - Efficient mapping for practical application
  - Flexible DMAC for efficient connectivity
  - Multiple clock sources and power saving modes
- **Quiet EMI/EMS**
  - Built-in noise cancellation, fewer components
- **Reliable and Secured**
  - Trusted flash and protection registers
  - Fail-safe features; oscillator-stop, non-stop WDT.

Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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ANALOG edge℠

# Designing Energy- Efficient Handheld Illumination Solutions

Application Note AN-1777

**Humair Khan,** Marketing Engineer

Portable battery sources are constantly challenged by the handheld applications' increasing functionality and power demands. By better understanding the applications' energy consumption, designers can produce energy-efficient solutions that will conserve battery life and provide a better end-user experience.

## Conserving Energy in Portable Displays

Display backlighting presents a significant energy challenge as handheld displays increase in size, resolution, and brightness. A typical small display module can require between three to ten LEDs for proper illumination.

To address the backlit display's energy consumption, one power-efficient method to drive LEDs is the switched capacitor. This technique connects the input voltage to a multiple-gain switched capacitor that produces a regulated output. The output voltage equals the gain multiplied by the input voltage during open loop operation. Closed loop operation enables a fixed output that should be slightly higher than the LED forward voltage and any voltage drop. The difference between output voltage and forward voltage is the headroom that needs to be monitored to ensure current flow. The switched capacitor remains in the most efficient gain over the widest input voltage consuming the least amount of energy through gain transitions that maintain regulation based on LED forward voltage and load requirements. Dual gain boost modes (1x and 3/2x for the LM2755 and LM2756; 2x and 3/2x for the LM2757) allow for the highest possible efficiency over a wide input voltage range resulting in longer battery life.

Consumer trends continue to dictate smaller portable devices, making PCB area much more valuable. The switched capacitor topology offers an added benefit as an inductor-less solution that saves on solution size and bill of materials. The LM2755, LM2756, and LM2757 are examples of switched capacitor boost technology that drive up to 10 LEDs (each driving up to 30 mA of diode current). This smaller solution provides the ability to place the driver in a local area, versus a central area, which reduces EMI.

Programmability of white LEDs is important to control display illumination. For example, when an end-user is having a conversation on a mobile phone, they are no longer interacting with the display, and the display has the option to dim. Both the LM2755 and LM2756 include an I²C-compatible interface that controls the display illumination based on handset operation.

***Figure 1*** shows the 32 exponential dimming step settings with an 800:1 dimming ratio which enables true perceived linear brightness level control and a dimming profile that leads to a smooth on/off display transition. The human eye is a logarithmic detector as it responds to light in terms of equal ratios rather than equal increments. What is recognized to be the linear augmentation of brightness is in reality exponential. By allowing the backlight to be dimmed or turned off, the designer gains flexibility and the ability to save battery life.

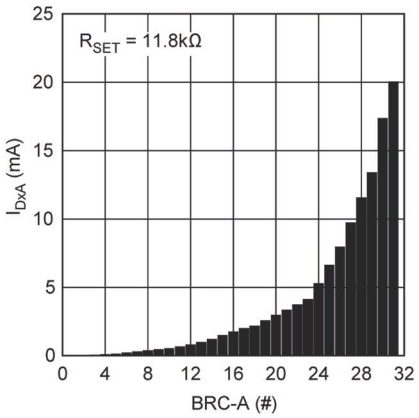


**Figure 1. 32 Exponential Brightness Levels**

***Figure 2*** is a typical application circuit of the LM2756. The LM2756 drives 8 LEDs separated in three independently controlled groups for multiple display purposes. Once the current level is set, analog current scaling internally dims the LEDs using the I²C-compatible interface. The 32 exponential analog brightness levels shown in ***Figure 1*** can be configured for the LEDs in Group A, while LEDs in Group B and Group C can handle 8 linear analog brightness levels.

With the ability to separately control several groups of LEDs, a single LED driver can control a main display,

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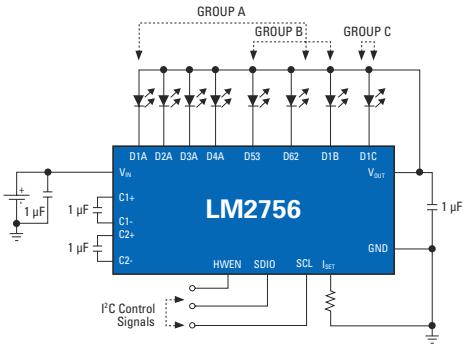


**Figure 2. LM2756 Typical Application Circuit**

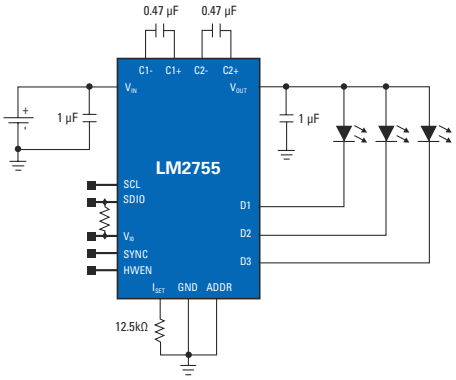


**Figure 3. LM2755 Typical Application Circuit**

a secondary sub-display or keypad LEDs, and an indicator LED. The LM2756 integrates these features by incorporating eight current sinks and dividing them into three groups. Four current sinks are comprised in Group A, while Group B and Group C have one current sink each. By manipulating a register, two extra sinks (D53 and D62) are available for either Group A or Group B. This allows 4, 5, or 6 LEDs to be used for the main display, leaving extra LEDs for additional lighting features.

## Peripheral Lighting

Personal mobile devices have greater illumination needs than just the main display. Supplemental LEDs are required for further lighting functions consuming more battery energy. Keypad lighting is an important characteristic of handheld applications that does not require as much LED current matching as current-sourced main display backlighting drivers. The LM2757 provides the smallest switched capacitor, voltage-sourced, boost solution to illuminate keypad LEDs with up to 90% efficiency. Indicator LEDs alert end-users of low battery, battery charging activity, and incoming messages. These LEDs can also be used in fun-lighting applications. With three independent RGB LED outputs, the LM2755 permits programmable blinking patterns, via I²C-compatible interface, for each output enabling multiple zone lighting.

For indicator and cosmetic lighting purposes, LEDs usually require a generated pattern. The LM2755, shown in ***Figure 3***, allows the designer to program a trapezoidal dimming waveform to independently control each output. The following equations calculate the durations of the delay, rise, fall, high, and low times shown on the waveform in ***Figure 4***:

$T_{STEP} = 50\mu s \times 2^{(N+1)}$ if using the internal clock

or $T_{STEP} = (1/f_{PWM}) \times 2^{(N+1)}$ if using the external clock on the SYNC pin

$$t_{rise/fall\ Total} = T_{STEP} \times (n_{high} - n_{low}) \times n_{Trise/fall},$$

where $0 \le n_{Trise/fall} \le 255$

$$t_{rise\ or\ fall\ Total} = 50\mu s \times (n_{high} - n_{low}),$$

where $n_{Trise/fall} = 0$

$$t_{high\ or\ low} = T_{STEP} \times (n_{high/low} + 1),$$

where $0 \le n_{Thigh/low} \le 255$

$$t_{delay} = T_{STEP} \times n_{delay},$$

where $0 \le n_{delay} \le 255$

The variables $n_{Trise}$, $n_{Tfall}$, $n_{Thigh}$, and $n_{Tlow}$ are numbers between 0 and 255 while $n_{high}$ and $n_{low}$ are selected numbers between 0 and 31 that become the brightness level boundaries when the dimming waveform enable bits are set to '1'. N is a number from 0 to 7 that is stored in the Time Step register. The PWM modulating signal period, $f_{PWM}$, is set to a default value of 50 µs. If using an external clock, this signal period becomes: $f_{PWM} = f_{SYNC}/32$. The custom waveforms only need to be programmed once for each output. After the values have been set, the I²C- compatible interface toggles start and stop times for the lighting pattern. Timing control features, like the one found in the LM2755, are an ideal tool for any peripheral lighting needs.

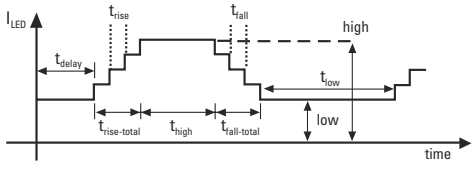


**Figure 4. LM2755 LED Timing Control**

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EDITED BY FRAN GRANVILLE

# pulse

INNOVATIONS & INNOVATORS

## 35-GHz waveform-analyzer plug-in triggers sequential-sampling DSO

Agilent Technologies has introduced a precision waveform analyzer in the form of a double-width plug-in for its model 86100C DCA-J (digital-communications analyzer)—an ultrahigh-bandwidth sequential equivalent-time-sampling DSO (digital-storage oscilloscope). Agilent designed the 86108A analyzer for engineers who verify and validate designs of high-speed electrical-communications systems and components. Residual jitter well below 100 fsec—which the company calls the industry's lowest—and channel bandwidths as high as 35 GHz ensure that users see the true performance of their signals.

Integrated instrumentation-grade hardware clock recovery greatly simplifies and speeds measurement setups, allowing the scope to trigger directly from single-ended or differential data signals and eliminating the need for a separate trigger input. Until now, says an Agilent spokesperson, a major headache for users of sequential-sampling DSOs has been finding and connecting a suitable trigger source without introducing delay that corrupts jitter measurements.

The integrated triggering system functions even in the presence of spread-spectrum clocking, allowing accurate signal analyses on components and systems in serial buses, such as PCI (peripheral-component-interconnect) Express and SATA (serial-advanced-technology attachment). An onboard phase detector enables the use of a simple, accurate technique based on clock or data inputs to measure jitter transfer and jitter/phase-noise spectra and to determine the PLL (phase-locked-loop) bandwidth of a device under test. US prices for the 86108A precision waveform analyzer start at $85,000.

**—by Dan Strassberg**

▷**Agilent Technologies,** www.agilent.com/find/dca.

### FEEDBACK LOOP

**"Back in the days when electronic-ignition systems were first used in cars, some makes would stall when a nearby mobile CB- or ham-radio operator keyed the transmitter."**

—Reader and frequent *Design Ideas* contributor Glen Chenier, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6515348. Add your comments.

Unlike other ultrawideband sequential-sampling scopes, the 86100C DCA-J with the 86108A precision-waveform-analyzer plug-in triggers from single-ended or differential data to produce eye diagrams with minimal residual internal jitter. You need not endure the hassle of locating and connecting a separate, stable, external trigger source.

# MEMS-oscillator maker aims to oust quartz

SiTime, which is bringing MEMS (microelectromechanical-system)-based oscillators into volume production, aims to replace quartz as the frequency reference in clock and timing oscillators. The company claims that its technology could potentially take over quartz's role in virtually all timing-oscillator sockets.

The company builds a small, square silicon-MEMS structure whose four side "beams" are suspended in free space; a cruciform shape spans the diagonals of the square, and a fixing point in the center suspends the structure. Under electrostatic excitation, the sides of the square flex in unison in the plane of the square, which measures only microns in size. The oscillation is at a fundamental frequency: In the products SiTime has so far released, this frequency is approximately 5 MHz, although the company has built structures that resonate from 1 to 40 MHz and above. The MEMS element exhibits high Q factor; the company says its design rules allow it to design for a given Q—of more than 70,000 in the commercial version.

The underlying technology originates with Bosch, and SiTime holds the rights to exploit it as a timing reference; related technology from Bosch Sensortec forms the basis of developments of the technology for use as a sensor.

This resonant structure features high mechanical robustness, has a stability in the parts-per-million range that is sufficient for the timing requirements of fast serial-data standards, and exhibits aging—frequency drift over time—that is smaller than that of all but the highest quality selected and preaged quartz crystals. It does not exhibit the typical frequency/temperature curve of a crystal but has a linear relationship that, in its oscillator products, SiTime compensates with an on-chip temperature sensor.

The company pairs its MEMS resonator with a CMOS programmable-frequency synthesizer chip. In its current product lineup, it assembles both dice in a multichip package to yield a fixed-frequency oscillator at 1 to 200 MHz. The company sets the programmed frequency by fuse programming before shipping. It could, says Marketing Vice President John McDonald, sell a user-programmable part, but a preprogrammed offering better conforms to the buying patterns in the supply chains for crystal oscillators. SiTime can program parts from stock to provide samples in days. The company aims to combine the MEMS element and the CMOS oscillator on a single

> A preprogrammed offering better conforms to the buying patterns in the supply chains for crystal oscillators.

die. It proposes to avoid difficulties inherent in a combined process flow by first building its MEMS structures and then carrying out the complete CMOS fabrication as a separate operation. The company anticipates the emergence of single-chip products in 2009; meanwhile, it has announced ultrathin and low-jitter versions of its oscillators.

The low-jitter part, SiT8102, has less-than-1-psec-rms phase jitter in most measurement bands, comes in a 2.5×2×8-mm QFN package, and will cost less than a comparable quartz device. You can use it as a clock reference for USB 2.0 HS, FireWire, Fibre Channel, SATA, PCI Express, Gigabit Ethernet, and other high-speed serial-communication protocols. In common with the company's other products, the construction uses a stacked-die arrangement; a temperature sensor on the CMOS-synthesizer chip is in close contact with the silicon of the resonator, sitting on top of it and allowing digital-temperature compensation. Although the chip applies compensation by changing division ratios, it is glitch-free, McDonald says. Total error is within ±50 ppm, including temperature and aging effects. Periodic jitter is less than 5 psec rms for most frequencies.

Removing the dice from the stacked layout and placing them side by side yields a thin oscillator that still has all of the mechanical-robustness attributes. The SiT8002UT is available with a 1- to 125-MHz output; requires a 1.8, 2.5, or 3.3V supply; and occupies a four-pin QFN package that measures 3×3.5×0.37 mm. The reduced thermal contact between the dice relaxes the device's stability over temperature of −40 to +85°C to ±100 ppm. Prices for the chips are less than $1 (high volumes). McDonald says that the manufacturing costs are inherently lower than those of quartz, which volume prices reflect.

SiTime's resonator technology does not achieve the close-in low-phase-noise specifications that digital-communications protocols demand. "We don't claim to be able to do the sort of high-RF-stability performance that is needed there; we are still perhaps 20 to 25 dB in phase noise away from that scenario," says McDonald. However, the company has achieved a better-than-15-dB improvement per year while developing the technology. McDonald also hints that the company may have the high-performance-quartz business in its sights.

**—by Graham Prophet**

▷**SiTime**, www.sitime.com.
▷**Bosch Sensortec**, www.bosch-sensortec.com.

DILBERT By Scott Adams

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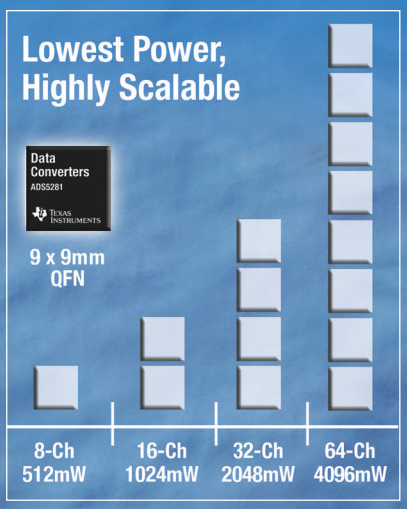


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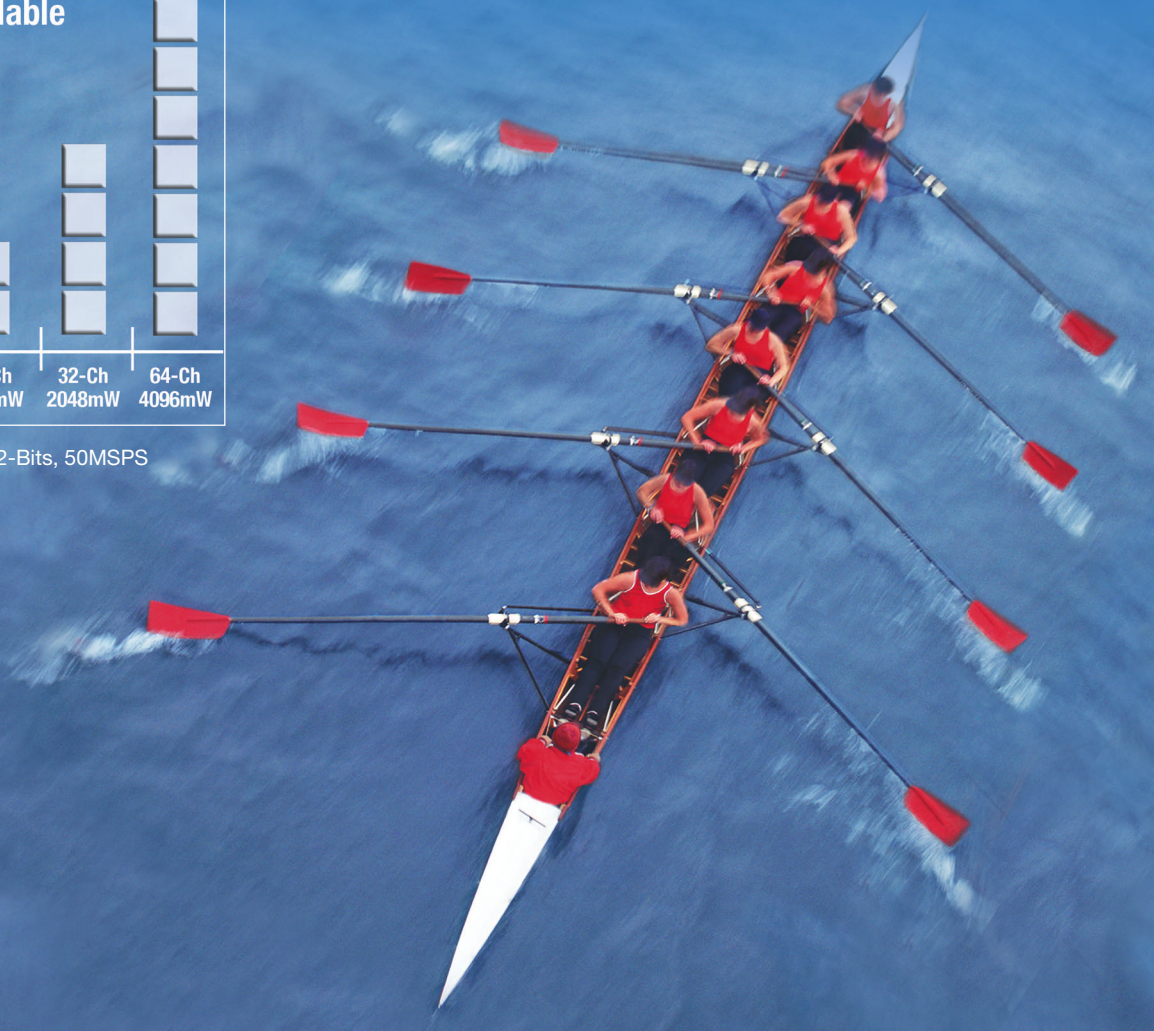


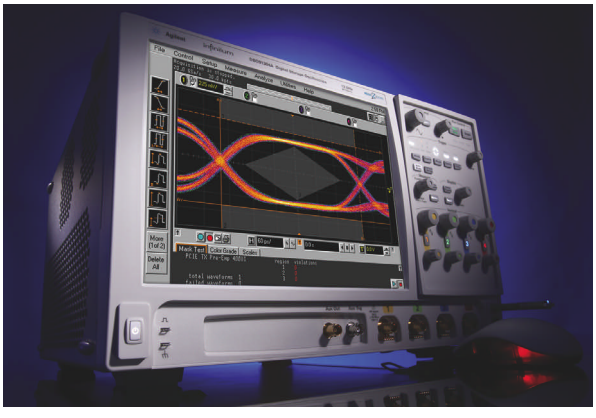
Texas Instruments

# Upgradable scopes capture 1G-sample records on all channels simultaneously

Agilent Technologies has announced a series of high-performance real-time-sampling DSOs (digital-storage oscilloscopes) that you can purchase with or upgrade to a waveform-memory depth of 1G samples on each of four channels. This record length is five times as great as that available in the deepest-memory competitive scope. The Infiniium 90000A Series also offers what the manufacturer calls the first integrated hardware/software-triggering system and the only three-level triggering system. InfiniiScan Plus, which identifies 150-psec hardware events, 75-psec software events, and 250-psec glitches, combines multiple hardware triggers with InfiniiScan software to provide virtually infinite trigger combinations for any debugging situation.

At the maximum acquisition rate of 40G samples/sec, which applies on all samples simultaneously, the new DSOs' optional ultradeep memory captures a 25-msec record on each channel. Proprietary data-accelerator technology enables the industry's fastest data offload, allowing rapid access to offline analysis. The new scope platform also provides Agilent's recognized ultralow timebase jitter and input noise. (For example, thanks to the company's RF-design expertise, proprietary-packaging technologies, and unique CMOS-ADC architecture, the 2.5-GHz-bandwidth unit offers a 147-µV-rms noise floor at 5-mV/division sensitivity.) Both the DSO and the DSA (digital-signal-analyzer) models can perform more than 150,000 measurements/sec and offer modes that support more than 300,000 triggers/sec.

The 90000A series includes 2.5-, 4-, 6-, 8-, 12-, and 13-GHz-bandwidth models with memory depths of 10M, 20M, 50M, 100M, 200M, 500M, and 1G samples/channel.



Infiniium 90000A oscilloscopes allow both bandwidth and memory upgrades. Any instrument is upgradable to the series maximum—13-GHz bandwidth and an industry-leading 1G-sample/channel acquisition-memory depth. Both figures apply to each channel, even with all channels active.

> "There is no penalty for waiting until you need it to purchase higher bandwidth.

Upgradable memory depth and the industry's only upgradable real-time-oscilloscope bandwidth and oscilloscope-application-server licensing protect your investment. What's more, if you buy a lower performance model and later upgrade it, your total cost will be the same as if you had initially purchased the higher performance; in other words, there is no penalty for waiting until you need it to purchase higher bandwidth. Agilent even changes the model-number labeling to match the upgraded performance. US prices for the series start at $29,000 and extend to $151,500 for the widest-bandwidth unit with the maximum possible memory.

**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/90000A.

# GPON-ONT IC delivers Gigabit Ethernet, voice, and video

Deployment of GPON (gigabit-passive-optical networks) is finally happening in North America with Verizon's drive to push fiber to the home (see "100-Mbps broadband: how, why, when, and where?" *EDN*, July 6, 2006, pg 48, www.edn.com/article/CA6347250). The passively split, shared fiber in a GPON deployment can deliver voice, video, and data. Now, chip companies, such as Iamba Networks, are focused on delivering ASSPs (application-specific standard products) to lower the cost of the customer-premises equipment. The company's new iSN1000 family of GPON ICs includes products targeting single-family homes, small businesses, and multi-dwelling units.

The iSN1000 chips implement the ONT (optical-network-terminal) function that serves as the interface between the GPON fiber and traditional twisted-pair, cable-TV, and Ethernet wiring in the home. Iamba based the iSN1000 family on three RISC cores and a traffic processor that the company calls the iTMP (Iamba traffic-pump module). The iTMP handles layer 2 and 3 network protocols at full wire speed and performs packet-classification, virtual-LAN, security, and IPTV (Internet Protocol-television) functions.

The iSN1000 provides two GbE (Gigabit Ethernet) ports and supports multiple voice and video lines. Iamba also offers a complete ONT-software package and a software package for the OLT (optical-line terminal) on the service-provider side of the GPON link. The iSN1000 ICs will sell for less than $20 (high volumes).

**—by Maury Wright**

▷**Iamba Networks**, www.iamba.com.

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TEXAS INSTRUMENTS

# Octal continuous-time sigma-delta ADC targets ultrasound and industrial applications

National Semiconductor is the first company to bring to market a high-speed, continuous-time sigma-delta converter. The 12-bit ADC12EU050 octal converter operates at 50M samples/sec and uses only 44 mW per channel. Whereas conventional sigma-delta converters use internal switched-capacitor filters, continuous-time converters use op-amp filters that offer resistive-input impedances. You face a trade-off for using this type of converter, however: You cannot vary sampling rates over a wide range because the parts must operate near 50M samples/sec. In addition to the resistive inputs, a major benefit of the architecture is low power consumption. Because of the nature of the architecture, it requires no input-sample-and-hold circuit.


National Semiconductor's continuous-time sigma-delta converters provide the speed of pipeline converters with the low power dissipation of conventional switched-capacitor sigma-delta converters.

Another benefit is single-clock recovery time from overloads. The SINAD (signal-to-noise-and-distortion) figure is 68 dB. The part operates from 1.2V, and you can drive the resistive inputs to a 2.1V p-p range.

Continuous-time delta-sigma converters have for 15 years been the subject of academic scrutiny. National Semiconductor's January 2007 acquisition of Xignal Technologies combined that company's advanced intellectual property with National Semiconductor's design, test, and manufacturing might. The company produces the part on a fine-line, 0.13-micron CMOS process from TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com). The part is the first in a line that will provide low-power, high-speed, 10- and 12-bit converters.

The devices have an internal low-jitter PLL (phase-locked loop) that cleans up and reduces the jitter of the applied clock signal while multiplying it by 16. The device uses this clock, divides it back down to the input frequency, and provides a pin for designers to use as a low-jitter system clock. A member of the company's Powerwise data-converter line, the part is available for sampling, and high-volume production will begin in the third quarter of this year. It comes in a 10×10-mm, 68-pin LLP and operates over a −40 to +85°C temperature range. The price is $64 (1000).**—by Paul Rako**

▷**National Semiconductor**, www.national.com.

## AMD UNVEILS 55-NM GRAPHICS PROCESSORS FOR LESS THAN $100

**02.21.08**

**With the aim of delivering outstanding graphics performance to the mainstream, AMD (Advanced Micro Devices) recently added the entry-level ATI Radeon HD 3400 and mainstream ATI Radeon HD 3600 graphics processors to its ATI Radeon HD 3000 series. Both processors integrate DisplayPort display connectivity, which allows the units to exceed current manufacturing expectations in the industry, according to the company.**

**The chips are part of AMD's first family of graphics cards using 55-nm manufacturing-process technology and allow users to view Blu-ray or HD DVDs in 1080p, thanks to AMD's UVD (unified-video-decoder) technology. The processors allow consumers to create immersive-home-theater environments using the built-in support for six-channel (5.1) Dolby Digital surround-audio transmission through an HDMI (high-definition-multimedia interface).**

**In addition, the ATI Radeon HD 3450 supports fully silent (passive) cooling for home-theater PCs. The processors allow twice the bandwidth of DVI (digital-video interface) due to the integrated DisplayPort support, which the company says allows low-cost, high-resolution, and bit-depth panels.**

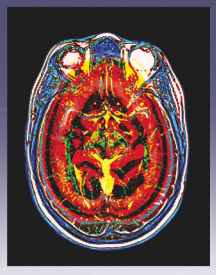
**Gamers looking for graphics processors that allow for further scalability will find that both series contain ATI CrossFireX, which adds the option of multiprocessor upgradability. ATI Hybrid Graphics will allow users to combine an ATI Radeon HD 3400 processor with a compatible AMD 7 series chip set to provide 3-D performance as part of the upcoming AMD mainstream high-definition "Cartwheel" desktop platform, adding further value to the gaming experience.**

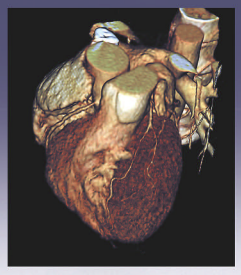
**Support for Microsoft DirectX 10.1 allows gamers to play HD games with 3-D graphics, realism, and shading effects, and PCI Express 2.0 support allows for twice the throughput of current PCI Express cards. The peak throughput of PCI Express 2.0 is 5 Gbps per lane in each direction versus 2.5 Gbps per lane in each direction for PCI Express 1.1. The ATI Radeon HD 3400 and ATI Radeon HD 3600 series cost $49 to $65 and $79 to $99, respectively.**

**—by Ann Steffora Mutschler**

**▶Advanced Micro Devices, www.amd.com.**

# ICs that enable world-class diagnostics for any patient, anywhere.







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ANALOG DEVICES

# VOICES

## GreenPeak Technologies' Cees Links: wireless-networking visionary

Cees (pronounced case) Links is an engineer and the chief executive officer at GreenPeak Technologies (www.greenpeak.com), an international supplier of low-power wireless-system modules compatible with IEEE 802.15.4 and ZigBee. Based in Utrecht, the Netherlands, Links has been a pioneer in the wireless industry and was involved in the establishment of the IEEE 802.11 standardization committee and the Wi-Fi Alliance. Links holds a bachelor's degree in electrical engineering and a master's degree in applied mathematics from Twente University of Technology (Enschede, Netherlands). The following is an excerpt of *EDN*'s interview with Links. For the full interview, go to www.edn.com/080221p1.

**Why did you select engineering and high technology as your profession?**

A As an engineer and manager, I am very fortunate to be able to combine creativity and innovation in my job. It is very exciting to watch products come to life, especially when these products have been designed by your own company. Whether it is software that goes live or a chip that is integrated into a laptop, seeing our products deployed in state-of-the-art products brings enormous job satisfaction. Creativity and the drive for true innovation are at the core of every high-tech-engineering job. I get a real thrill knowing that thousands of people use my company's Wi-Fi chips in their laptops every day. Bringing comfort to people's everyday lives is a bonus.

**What is your vision for the future of wireless-networking technology?**

A Many people are not aware of the tremendous waste of energy in our environment and the tremendous opportunity for conserving that energy. For example, lights can be switched off when no one is in a room, and temperature can be lowered when employees are not using a meeting room. With the help of sensor networks, consumers and plant managers can better identify wasteful energy use and institute automated procedures, like switching off lights and lowering temperature, that facilitate the design of smarter, more efficient homes, buildings, and industrial plants.

> The biggest technical challenge is managing energy consumption without reducing range or functionality.

Until now, wires and cables have limited the widespread adoption of sensor networks by making them difficult and expensive to install and maintain. Wireless alternatives have emerged that simplify installation and reduce cost. But high power consumption and the corresponding need for regular battery replacement have made these wireless networks difficult and costly to maintain.

To combat this problem and facilitate the widespread deployment of wireless-sensor networks, GreenPeak has developed an ultralow-power-communication technology that uses energy harvested from the environment. GreenPeak's wireless technology is also self-forming and self-healing, which simplifies installation.

GreenPeak's long-term vision is to build a smarter world by developing a communications platform with advanced sensing-interfacing capability that enables us to better control our lives, homes, and environment. We believe that, in a connected world, people can live in a more comfortable and safer environment with less energy waste.

**What are the biggest technical challenges in achieving your vision?**

A The sensors used in wireless-sensor networks are often small and cannot hold large batteries. As a result, the batteries must be regularly replaced, which creates a real maintenance headache. GreenPeak has overcome this problem by developing alternative solutions for powering wireless-sensor networks based on a different and low-power architecture that can use energy harvested from the environment. The biggest technical challenge is managing energy consumption without reducing range or functionality, like speed and standards compliance.

**How will ultralow-power-network technologies further develop?**

A Low-power technology for wireless-sensor and -control networks will evolve in several stages. In the first stage, wireless-sensor networks will replace standard wired implementations, thereby making sensor networks much easier to install and significantly less expensive. Eliminating battery replacement will also simplify maintenance and provide a higher level of safety and comfort, which will enable ultralow-power wireless-sensor networks to find widespread adoption in home, office, and industrial settings.

**What are your favorite leisure-time activities?**

A I am happily married and have three daughters and a son. It is important to me to spend as much time with my family as possible or play the piano and enjoy a glass of wine. I also play in the local volleyball competition, where I enjoy playing and winning as a team, and I also love a strategic game of chess.

**—by Warren Webb**

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BY BONNIE BAKER

# Delta-sigma ADCs in a nutshell, part 3: the digital/decimator filter

Following the modulator in the delta-sigma ADC is a digital/decimator circuit. This circuit samples and filters the modulator stream of 1-bit codes. At the modulator output, high-frequency noise and high-speed sample rates are problems. However, because the signal now resides in the digital domain, you can apply a digital-filter function to attenuate the noise and a decimator function to slow the output data rate. Designers often intertwine the digital filter and decimator functions in the same silicon.

**Figure 1** shows the signal as it travels through the digital/decimator-filter functions. The digital-filter function operates at the same rate as the modulator sampling rate (**Figure 1a**). Notice that the 24-bit code-train resembles the original signal (**references 1** and **2**). In the time domain, it looks like the digital-filter function is responsible for the low noise and high resolution of the delta-sigma converter. However, this function provides a second-order impact on the system noise by rejecting higher frequency noise, where the noise shaping from the modulator dominates noise reduction in the lower frequency band (**Figure 1b**).

The digital-filter function provides a digital version of the input, but the data rate is still too fast to be useful. Although it might appear that you have an abundance of high-quality, multibit samples at a high sampling rate, you don't need most of this data.

The second function of the digital/decimator filter is the decimator. Decimation is the process of reducing a digital signal's output rate to the system's Nyquist frequency. One simple way to implement a decimating function is to average together groups of 24-bit codes (**Figure 1c**). The decimator accumulates these high-resolution data words, averages several words together, outputs the average results, and dumps the data for the next average. A more economical way to implement a low-power decimator function is to simply pick out a 24-bit word every Kth sample without performing additional averaging. (K is equal to the oversampling or decimation ratio.)

Almost all delta-sigma converters incorporate a class of averaging filters called sinc or FIR filters, named for their frequency response. Many delta-sigma devices use other filters with sinc filters for two-stage decimation. Low-speed industrial delta-sigma ADCs usually use only a sinc filter.

In the frequency domain, you can see that this digital/decimator filter simply applies a lowpass filter to the signal (**Figure 1b**). In so doing, the digital/decimator filter has attenuated the higher frequency-modulator quantization noise. With the reduced quantization noise, the signal re-emerges in the time domain. EDN

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2. Baker, Bonnie, "Delta-sigma ADCs in a nutshell, part 2: the modulator," *EDN*, Jan 24, 2008, pg 24, www.edn.com/article/CA6518678.
3. Baker, R Jacob, *CMOS Mixed-Signal Circuit Design*, J Wiley & Sons, ISBN 0471227544.


*Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.*

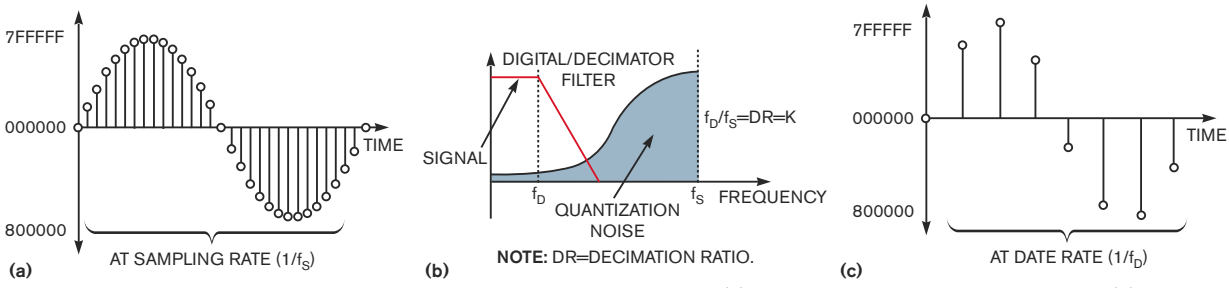


Figure 1 The digital-filter output function produces a high-resolution result (a), while rejecting high-frequency noise (b). The decimator function slows the output data rate (c).

# Design with the best: Power Management

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

# What does "better" mean?

Since the days of Scottish inventor and engineer James Watt, engineering practice has focused on balancing multiple goals: improving performance, increasing robustness, expanding function, and reducing cost. As has been the case for the two centuries since Watt, the market decides for each product the value of any particular combination of these four attributes. Alas, thus far, no one has extracted a useful value predictor from the historic market data.

Engineers can and do observe market behaviors, however, and they glean trends that help inform engineering judgments. During the last 20 years or more, the trend in consumer products has been to push the balance to favor cost reduction, product-function expansion, and performance improvement, often at the cost of robustness. The assumption has been that rapid advances in technology will render products obsolete before their marginal robustness becomes an issue. As successful as this strategy has been, its usefulness may be running out for two reasons.

A number of consumer products have evolved to the point at which existing performance levels and features are entirely adequate for most users. Further efforts to increase value along these two axes may not enjoy correspondingly greater traction in the market.

For example, a low-end home computer selling for a fifth of the original IBM model 5150 PC's price operates with a clock nearly three orders of magnitude faster, a dual-core processor with eight times wider datapaths, and four orders of magnitude larger memory. A direct comparison of the two machines is not the point. Consider these devices rather as milestones, with many in between, measuring the progress the industry has made during 26 years of innovation. The market's response to this innovation has been tremendous. Consider, however, how customers might value a doubling of any of the machine's capabilities. Can household customers benefit from a further doubling of clock speed or disk space? Would four cores change their typical experience enough to justify the expense?

**Once a machine's capabilities are sufficient that they no longer limit the customer's use, the incremental value of increasing capability sharply drops.**

Once a machine's capabilities are sufficient that they no longer limit the customer's use, the incremental value of increasing capability sharply drops. This situation is true of home computers as well as mobile handsets, home-entertainment equipment, appliances, and a host of other products.

As more products reach this point, at which typical models are entirely adequate to meet the market's needs, product robustness—or a lack thereof—becomes more conspicuous. This concept is particularly true in this modern age of so-called viral marketing. In this environment, the picks and pans of ordinary users can influence purchasing decisions more effectively than can your company's advertising efforts—particularly the pans.

Nothing taints a customer's otherwise positive experience of a product or his or her assessment of its manufacturer more than a failure within the device's expected lifetime. Common failures for consumer and portable devices include failures of electromechanical parts, such as switches, keypads, and connectors. ESD (electrostatic discharge) and power-supply surges induce another common class of failure mode. Rarely do I hear of consumer electronics failing at the core function. Rather, it's at the device's periphery—the bits that stand between the functional core and the outside world—where one often finds the products' weaknesses and opportunities to make products better. EDN

*Joshua Israelsohn is a co-founder of JAS Technical Media, where he manages the company's technical-communication-consultancy practice. He holds an SBEE from the Massachusetts Institute of Technology (Cambridge) and has more than 15 years of design experience. You may contact him at jisraelsohn@ieee.org.*

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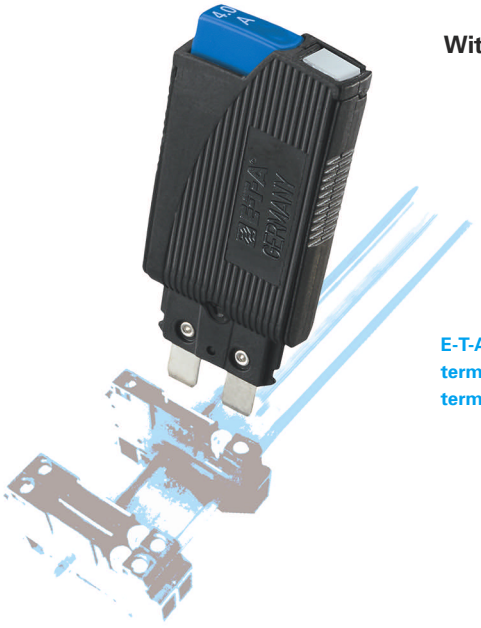


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**Go to www.edn.com/080221pry for an expanded write-up of Picturevision, complete with additional photos.**

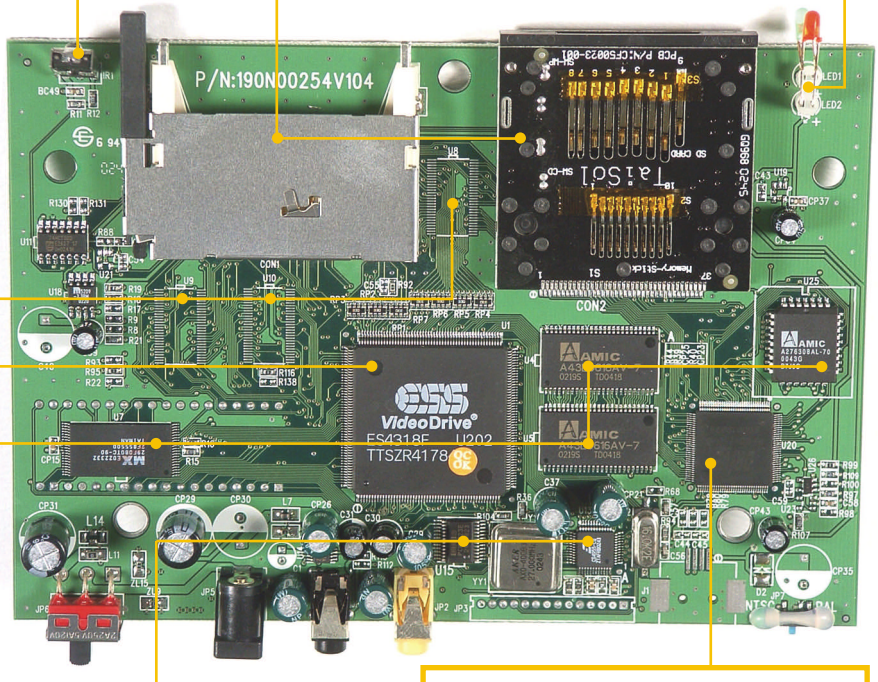
# TV peripheral encompasses superset processor

In September 2002, Delkin (www.delkin.com) introduced its eFilm Picturevision, which enables the playback of audio, still-image, and video files on a variety of memory-card formats. The price was then $159; by April 2004, the price was down to $9.99 after a $50 rebate. The device includes many hardware building blocks that enable it to work its decoding and displaying magic.

The system design contains many elements of mystery. For example, the PCB has unpopulated sites for three additional SOP-enclosed ICs, along with unused locations for numerous capacitors, inductors, and resistors.

Delkin's product natively handles CompactFlash I and II, including MicroDrive; Memory Stick, but not higher capacity Memory Stick Pro; Multimedia Card; Secure Digital, but not higher capacity SDHC (secure-digital high-capacity); and now-defunct SmartMedia module formats. Front-panel LEDs indicate valid system power and in-progress memory-card accesses. On the other end of the front panel, you'll find an infrared receiver that partners with the supplied remote control.

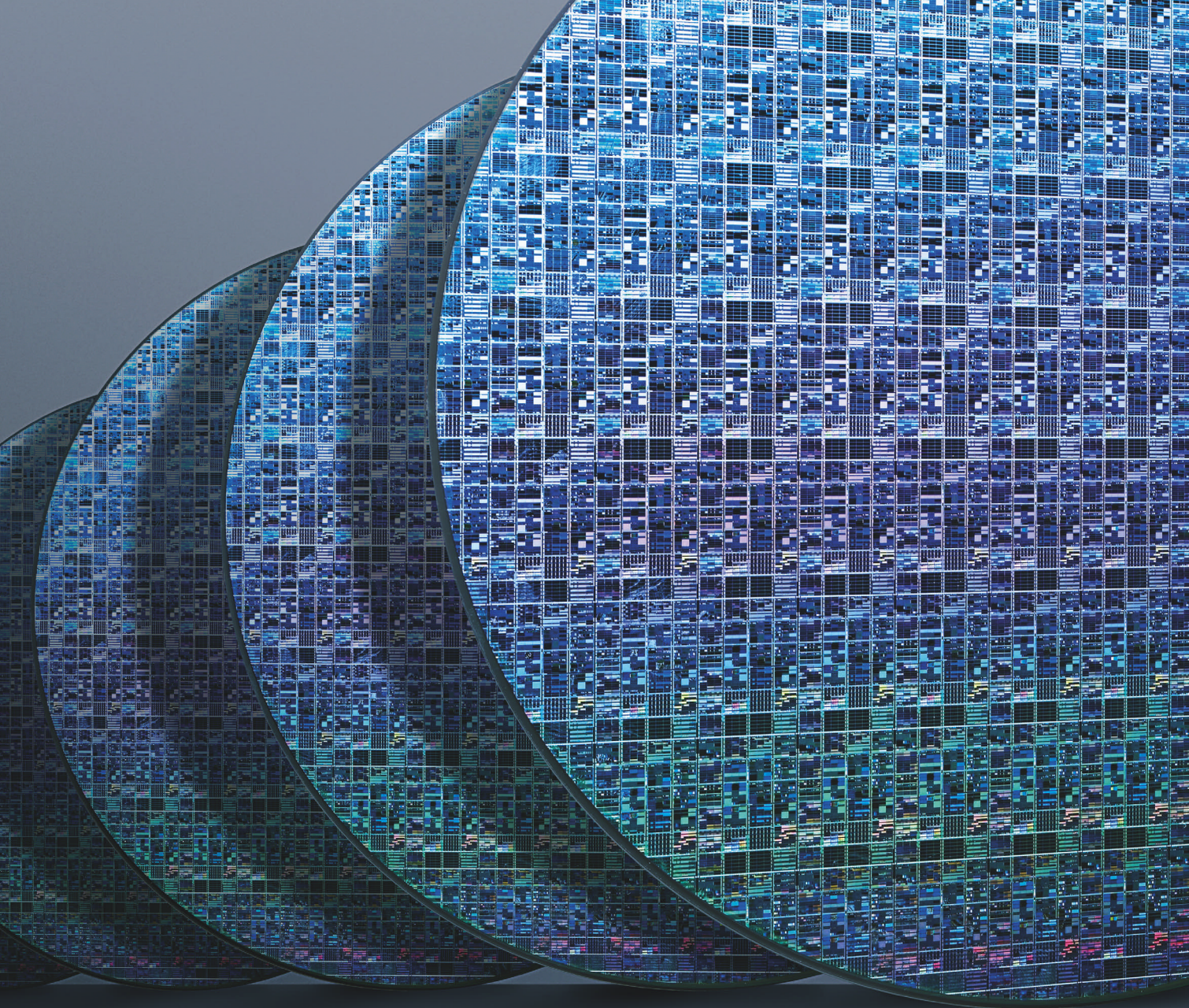
The heart of Picturevision is ESS Technology's ES4318 DVD processor. This 208-lead, PQFP-enclosed IC tackles JPEG images, MP3 audio tracks, and MPEG-1 and MPEG-2 video clips on behalf of Delkin's device. But, the ESS IC can support many other formats. Picturevision is a case study of the appeal of leveraging high-volume and, therefore, low-cost semiconductors.




Picturevision's memory foundation comprises a curious mix of three technologies: Macronix's 8-Mbit 29F080 flash memory, AMIC Technology's 512-kbit, OTP A276308 EPROM, and two 16-bit AMIC A43L0616 SDRAMs. Proximity and trace routing suggest that the 29F080 houses code that the ES4318 executes, but what of the seemingly redundant nonvolatile A276308? Does it store overflow code for the ES4318 that, by virtue of its EPROM location, you can't update within the system? Does it hold nonupgradable system data? Or is it the nonvolatile-memory partner to another system IC? And where is the EEPROM or battery-backed SRAM? Maybe this design needs no nonvolatile, byte-rewritable storage.

Cirrus Logic's CS4955 video encoder combines with an NTSC/PAL switch on the system back panel to convert the ES4318's digital-video output into a composite analog-video connection. Similarly, Texas Instruments' PCM1723 DAC with integrated PLL translates the ES4318's I²S audio interface into two-channel analog audio.

Consider, too, the mysterious QFP chip with the word "DRiVE" stamped in large type on the first line of the package mark, "free" below it, and "PF08-2-0-0" on line three. No amount of Google searching uncovered the chip's identity, and those at Delkin who might know the answer have long ago departed. My guess is that it's an interface chip that translates between Picturevision's various memory-card slots and the ATAPI (advanced-technology-attachment-packet-interface) port that the ESS ES4318 expects.



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- Agilent Technologies — See Avago Technologies
- Agilent Technologies Test Equipment
- AIM Electronics — See Emerson Network Power
- Akro-Mils
- Alcoswitch — See Tyco Electronics
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- Alpha Wire
- Altech Corp.
- American Beauty
- American Electrical, Inc.
- American Power Conversion (APC)
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- Angstrohm/Vishay
- APC — See American Power Conversion
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- APM Hexseal
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- Aromat — See Panasonic Electric Works
- Aromat Controls — See Panasonic Electric Works
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- Ault Incorporated — See SL Power
- Automatic Timing & Controls — See ATC
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- AVX
- Axicom — See Tyco Electronics
- AZ Displays, Inc.

## B

- Banner Engineering
- BCcomponents/Vishay
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- BK Precision
- Bogen Communications, Inc.
- Bomar Interconnect Products
- Bourns
- Box Enclosures
- Brother International
- Buchanan — See Tyco Electronics
- Bud Industries
- Bulgin Components, plc
- Bussmann — See Cooper Bussmann

## C

- C&K Components
- C.K Tools
- Caddock
- Cambridge Products — See Emerson Network Power
- Carling Technologies
- Carlo Gavazzi, Inc.
- Cera-Mite/Vishay
- Chemtronics — See ITW/Chemtronics
- Cherry Electrical Products, Inc.
- Chicago Miniature Lamp — See CML Innovative Technologies
- CII — See Tyco Electronics
- Cinch
- Clarostat — See Honeywell/Clarostat
- CML Innovative Technologies
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- Collmer.com — See HVCA
- Comair Rotron
- Condor — See SL Power
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- Cooper Bussmann
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- Copal Electronics — See Nidec Copal Electronics
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- Crouzet
- Crydom Inc.
- **Crystek Crystals Corp.***
- CSI/Speco — See Speco Technologies
- Custom Connector
- Cynergy3 Components

## D

- Dale/Vishay
- Dallas Semiconductor
- Danaher/Veeder-Root
- Dantona Industries, Inc.
- Davies Molding
- Dearborn — See Manhattan Wire Products
- Desco
- Dialight
- Diversified Electronics — See ATC
- Draloric/Vishay
- Duracell
- Dymo — See Also RHINO

## E

- E-T-A Circuit Protection & Control
- Eagle Picher
- EAO Switch
- Eaton/Commercial Controls
- Eaton/Heinemann
- ebm-papst
- EBT Optronic — See CML Innovative Technologies
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- Electrix
- Electrocorp — See Honeywell/Electrocorp
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- HARTING Elektronik
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- igus
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- International Rectifier
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- Itailiana/Vishay
- ITT/Cannon — See C&K Components
- ITW/Chemtronics

## J

- JAE Electronics, Inc.
- Johnson Components, Inc. — See Emerson Network Power
- Jonard — See OK Industries

## K

- K-Sun
- KEMET
- Kester Solder
- Keystone Electronics
- Keystone Thermometrics — See GE Infrastructure Sensing
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- Kilovac — See Tyco Electronics
- Klein Tools
- Kroy, Inc.

## L

- L-com Connectivity Products
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- Lascar Electronics
- Lattice Semiconductor
- Leecraft — See Lighting Components and Design
- Lighting Components and Design
- Linemaster
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## M

- Macromatic
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- Power-Sonic
- Primary Power Components (PPC) — See Qualtek Electronics Corp.
- Products Unlimited — See Tyco Electronics

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- Q-Cee's — See Tyco Electronics
- Qualtek Electronics Corp.
- Quest Technology International, Inc.

## R

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- **Recom***
- Red Lion Controls
- Redington Counters, Inc.
- RHINO — See Also Dymo
- Richco
- Roederstein/Vishay
- Rotron — See Comair Rotron
- Ruland

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- SanDisk
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- Schaffner
- Schrack — See Tyco Electronics
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- Selco
- SemiKron
- Sensotec — See Honeywell/Sensotec
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- Spectra•Strip/ITD — See Amphenol
- Spectrol/Vishay
- Sprague/Vishay
- SRC Devices
- SSP/Vishay
- Staco Energy Products Co.
- Stancor/White-Rodgers
- Steinel
- Sti (Scientific Technologies Inc.) — See Omron STI
- STMicroelectronics
- Storm Interface
- Streamlight
- Struthers-Dunn
- Sunbrite — See Lumex
- Sunon Fans
- SunX/Aromat – See Panasonic Electric Works/Sunx
- Superior Electric
- SurgX — See Cooper Bussmann
- Switchcraft
- Sypris Test & Measurement — See F.W. Bell

## T

- Tadiran
- Tapeswitch
- Techspray
- Techno/Vishay
- TEKO
- Tektronix
- Teledyne Relays
- Telemecanique
- Texas Instruments
- Thermometrics — See GE Infrastructure Sensing
- Thin Film/Vishay
- Thomas & Betts
- Thordarson Meissner
- Time Mark Corporation
- Toshiba
- Triad Magnetics
- Tripp Lite
- TURCK
- Twin Industries
- Tyco Electronics
- Tyton Hellermann — See HellermannTyton

## U

- Ultronix/Vishay

## V

- Vector Electronics & Technology
- Viewsonics — See Emerson Network Power
- Vishay
- Vishay Semiconductors
- Vitramon/Vishay
- Volex Power Cords

## W

- Waber by Tripp Lite
- WECO
- Weller — See Cooper Tools
- White-Rodgers
- Wire Pro, Inc. — See WPI
- Wiremold
- WPI

## X

- Xcelite — See Cooper Tools
- Xicor
- Xilinx

## Y

- Yuasa — See EnerSys

## Z

- Zettler Magnetics

*New Supplier



# ANALOG-TO-DIGITAL CONVERTER ICs

YOUR SEMICONDUCTOR SOLUTIONS RESOURCE

Volume 8, Issue 1

## Contents



analog is everywhere.™

*Get answers to some of* ***engineering's toughest questions*** *in this collection from ADI*


## High Speed, High Accuracy, Low Power ADCs for Efficient Precision Control

Today's designs for motor control and automotive applications require ADCs that have high speed to digitize auxiliary input/output signals, real-time results output to the processor, and simultaneous sampling to maintain correct phase information. Meeting these needs in a compact footprint is a challenge faced by all IC suppliers.

### *Solution*

The AD7356 12-bit, 5 MSPS, dual-channel simultaneous sampling ADC is unlike any other SAR ADC that ADI offers. It is 25% faster than other single-channel SAR ADCs in the 12-bit resolution range and 3× faster than the next fastest simultaneous sampling SAR ADC.


**APPLICATIONS**

- Industrial motion control
- Adaptive cruise control (ACC)
- RFID transceivers

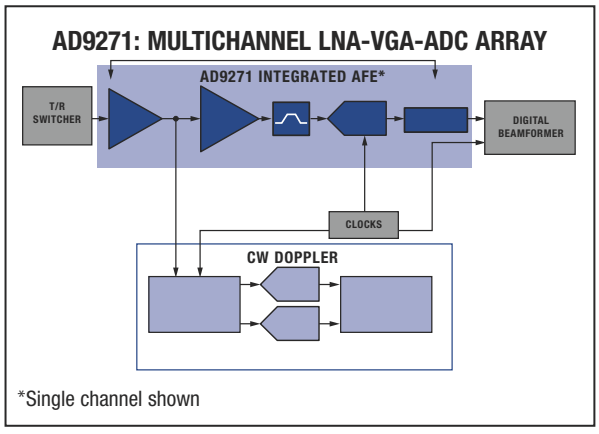
The higher data throughput rate offered by the AD7356, with no limitation on time between conversions, provides a key performance advantage for devices where continuous measurement of motor functions is required to maintain precision operation. One such application is optical encoders used in high speed industrial motor controls. ADI also offers an extended portfolio of high performance products offering lower speed or increased channel count to suit all design needs. Pair ADI's AD8022 ADC driver with the AD7356 for optimal low noise driving.

| Product | Description | Power Dissipation (mW)* | Package | Price ($U.S.) |
|---|---|---|---|---|
| AD7356 | Dual, 5 MSPS, 12-bit, 1-channel | 35 | 16-lead TSSOP | 7.89 |
| AD7357 | Dual, 4.25 MSPS, 14-bit, 1-channel | 38 | 16-lead TSSOP | 10.81 |
| AD7276 | Single, 3 MSPS, 12-bit, 1-channel | 12.6 | 6-lead TSOT | 6.25 |
| AD7266 | Dual, 2 MSPS, 12-bit, 3-channel | 27 | 32-lead LFCSP, 32-lead TQFP | 7.55 |
| AD7265 | Dual, 1 MSPS, 12-bit, 3-channel | 17 | 32-lead LFCSP, 32-lead TQFP | 5.75 |
| AD7866 | Dual, 1 MSPS, 12-bit, 2-channel | 18 | 20-lead TSSOP | 5.95 |

*Typical power dissipation.

## Integrated Analog Front End (AFE) Contains Eight Ultrasound Receive Channels in a Single IC

The AD9271 delivers an unprecedented level of integration for cart-based and portable ultrasound designers. Each of the eight channels features a low noise amplifier (LNA), an 8 × 6 differential crosspoint switch for continuous wave (CW) Doppler, a variable gain amplifier (VGA), an antialiasing filter (AAF), and a 12-bit analog-to-digital converter (ADC). The AD9271 operates on a 1.8 V supply, consuming only 150 mW/channel at 50 MSPS. With eight channels in a 16 mm × 16 mm, 100-lead TQFP, the AD9271 allows ultrasound system designers to increase their channel count and image quality without increasing the size or power consumption of the equipment.




AD9271-25 $40.00

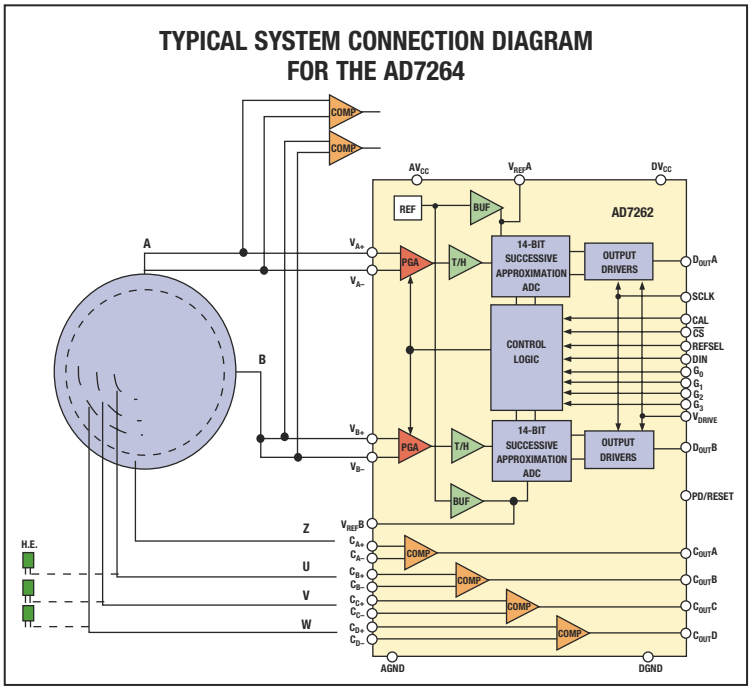
By integrating high performance elements into a single IC, superior image quality is enabled on portable and cart-based ultrasound systems used in emergency rooms, doctors' offices, and clinics. Each channel of the AD9271 features a variable gain range of 30 dB, typical input referred noise of 1.2 nV/√Hz @ 5 MHz, input dynamic range of 157 dB/√Hz, a programmable third-order Butterworth antialiasing filter, a 12-bit ADC with an SNR of 70 dB, and spurious-free dynamic range (SFDR) of 80 dB. It is possible to power down individual channels to extend battery life during display mode only, or to power down the data conversion path when using the LNA in CW mode.

## Dual, Simultaneous Sampling, 14-Bit, 1 MSPS, Low Power SAR ADC for Motor Control

Approximately 70% of the electricity generated globally is used to run motors. More efficient motor drives reduce power consumption—leading to substantial energy savings. ADI has produced a range of products that may be used to ensure that motors are more efficient. Our portfolio includes the AD7264, a true differential, dual, 1 MSPS, 14-bit, 2-channel ADC that acquires motor shaft position information from a shaft encoder. This system on a chip simplifies industrial motor control designs by integrating two successive approximation (SAR) ADCs, a programmable gain amplifier (PGA), and four comparators on a single IC. By providing a direct interface for multiple types of sensors, this new ADC solution allows a single, standardized data acquisition board for industrial motor drives, replacing as many as three separate boards as was previously required. This integration allows designers to develop simpler, more cost-effective, and efficient motor control units.

The integrated PGA has a flexible gain setting from 1 to 128, which can be used to interface directly to a variety of encoders without requiring any additional circuitry. Also included on chip are four comparators. Three of these comparators can be used to monitor Hall effect pole sensors from a magnetic encoder or the inner tracks from an optical encoder. The fourth is used as a reference or "Z" marker.

Offset and gain calibration registers can be used for device or system offset and gain calibration. The device features a variety of power-down options that allow users to optimize their power dissipation for different system requirements. Power-down options and PGA gain settings can be selected via the dedicated device pins or by writing directly to the device. ADI's AD8132 and ADA4941-1 are recommended drivers for single-ended and differential conversion.



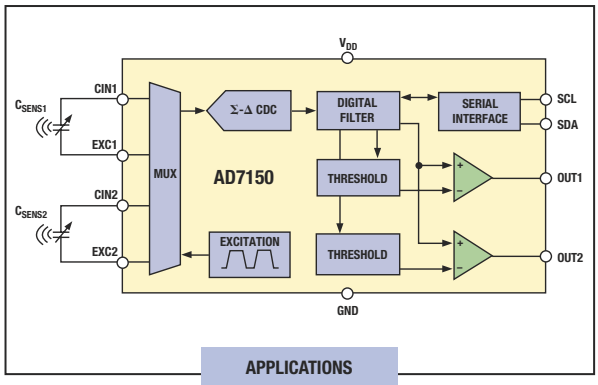

AD7264 $7.50
AD8132 $1.65
ADA4941-1 $2.39

**FREE OFFER**
Samples and Data Sheets

**www.analog.com/V8ADC**

## ADI Delivers Ultralow Power, High Sensitivity, and Fast Proximity Detection

Detecting proximity with capacitance sensors is no easy task. Most applications focus on a particular performance requirement—power, for example. However, speed and sensitivity are also very important as they have a large bearing on the detection response time and the detection distance, respectively. In most cases, compromise cannot be tolerated on either of these three important specifications. Unfortunately, current solutions on the market focus on one of these three important requirements, but fail to deliver performance on the other two requirements.




**APPLICATIONS**
- Proximity sensing
- Position detection
- Contactless switching

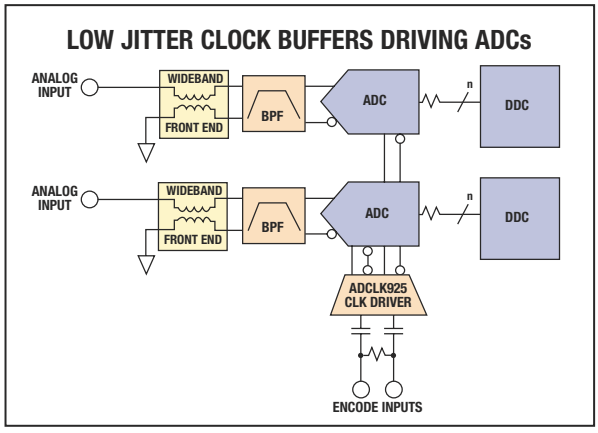
| | |
|---|---|
| AD7150 | $1.35 |
| AD7151 | $1.35 |

By using Analog Devices' state-of-the-art Σ-Δ ADC architectures, the AD7150 and AD7151 detect proximity without compromising power, sensitivity, or speed. Ultralow current consumption of 70 μA is delivered with a sensitivity of 1 fF and a detection speed of 10 ms. With a comparable sensitivity, the nearest competing device has a detection speed of 30 ms at a near 10× current consumption of 600 μA. The AD7150 and AD7151 also feature an on-chip adaptive environmental algorithm, which automatically compensates for drifts in the capacitance sensor due to temperature, humidity, dust, and dirt.

| Part Number | Number of Channels | Current Consumption (μA) | Sensitivity (fF) | Speed/ Response Time (ms) | Max Sensor Capacitance $C_{SENS}$ (pF) | Interface | Package | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| AD7150 | 2 | 100 | 1 | 10 | 13 | I²C® | 10-lead MSOP | –40 to +85 |
| AD7151 | 1 | 70 | 1 | 10 | 13 | I²C | 10-lead MSOP | –40 to +85 |

## Low Jitter Clock Buffers Improve ADC Performance

High speed, high performance ADCs are now able to sample very high frequency signals with great accuracy. To do so reliably, however, requires an extremely low jitter clock source at the ADC encode pins.




The diagram on the right shows how the new 1:2 ECL clock buffer, the ADCLK925, may be used to deliver a low jitter encode clock to two ADCs. Because the ADCLK925 features random rms jitter of less than 100 femtoseconds (fs), the resulting ADC signal-to-noise ratio (SNR) typically improves by 12 dB as compared with circuits with 400 fs of clock jitter. Also, the integration of two clock buffers on a single chip ensures that the delay skew between clock A and clock B will be negligible. Fast output rise and fall times of 60 ps maximize bandwidth and signal integrity. Any extra SNR realized in the ADC stage is passed on to digital processing chips, such as digital downconverters (DDCs). These digital filters are more accurate and predictable than their analog equivalents. The overall benefit to the system designer is a smaller, lower cost, higher performing digitizer circuit.

| Part Number | Number of Inputs | Max Clock Input (GHz) | Number of Outputs | Max Clock Output (MHz) | Price ($U.S.) |
|---|---|---|---|---|---|
| ADCLK905 | 1 | 6 | 1 | 6000 (ECL, PECL, LVPECL) | 5.60 |
| ADCLK907 | 2 | 6 | 2 | 6000 (ECL, PECL, LVPECL) | 7.95 |
| ADCLK914 | 1 | 2.5 | 1 | 2500 (HVDS) | 6.95 |
| ADCLK925 | 1 | 6 | 2 | 6000 (ECL, PECL, LVPECL) | 6.95 |

**For samples and data sheets, visit www.analog.com/V8ADC**

## Multichannel ADCs Reduce Power and Space Requirements

As data acquisition designers are challenged to deliver solutions that provide the greatest accuracy with the highest integration and lowest power, multichannel ADCs have become an increasingly popular choice. The AD768x family of 14-bit and 16-bit ADCs meets all of these requirements with added features to further simplify design cycles.

The AD7699 is the fastest 16-bit, 8-channel ADC at 500 kSPS. Both the AD7682 and AD7689 provide 2.7 V operation to save on power. The 14-bit AD7949 provides 8-channel operation at low cost. Other family features include a configurable multiplexer that allows for single-ended, differential, or bipolar input signals, a selectable voltage reference (2.5 V or 4.096 V), a temperature sensor, a selectable one-pole filter, and a sequencer to allow continuous scanning of channels. Recommended driver amplifiers for the AD768x family include the ADA4841-2, AD8021, and AD8022.

| Part Number | Channels | Resolution (Bits) | Sampling Rate (kSPS) | INL Error (ppm) | Voltage Supply (V) | Price ($U.S.) |
|---|---|---|---|---|---|---|
| AD7682 | 4 | 16 | 250 | 30 | 2.7 to 5 | 4.80 |
| AD7689 | 8 | 16 | 250 | 30 | 2.7 to 5 | 6.99 |
| AD7699 | 8 | 16 | 500 | 30 | 5 | 7.99 |
| AD7949 | 8 | 14 | 250 | 60 | 2.7 to 5 | 3.99 |

## 24-Bit Oversampling ADCs for Low Power Equipment

ADI's 24-bit oversampling ADCs were designed to extend the Σ-Δ portfolio beyond the output data rates of the industrial type Σ-Δ ADCs.

These ADCs combine the benefits of a large dynamic range and input bandwidth and, in the case of the AD7766 and AD7767, low power for high end instrumentation applications such as vibration analysis, sonar, and audio. In applications where small changes on the input are measured on larger ac or dc signals, the AD776X product family is the perfect design fit. Recommended complementary ADI products for the AD776x family include the ADA4841 low noise and distortion rail-to-rail output amplifier, and the ADA4941 low power, low distortion, high SNR driver amplifier.


**APPLICATIONS**

- Data acquisition
- Vibration analysis
- Bearing monitoring
- Radio and HF radio
- Sonar

| Part Number | Dynamic Range (dB) | Max Output Data Rate | Programmable Oversampling Rate | Interface | Package | Low Power Mode (mW) | Price ($U.S.) |
|---|---|---|---|---|---|---|---|
| AD7760 | 120 | 2.5 MSPS | 8× to 256× | 16-bit parallel | 64-lead TQFP | 661 | 34.95 |
| AD7762 | 120 | 625 kSPS | 32× to 256× | 16-bit parallel | 64-lead TQFP | 661 | 17.95 |
| AD7763 | 120 | 625 kSPS | 32× to 256× | Serial | 64-lead TQFP | 651 | 17.95 |
| AD7764 | 115 | 312 kSPS | 64×, 128×, 256× | Serial | 28-lead TSSOP | 160 | 13.95 |
| AD7765 | 115 | 156 kSPS | 128×, 256× | Serial | 28-lead TSSOP | 160 | 8.95 |
| AD7766 | 109.5 | 128 kSPS | 8× | Serial | 16-lead TSSOP | 15 | 5.95 |
| AD7766-1 | 112.5 | 64 kSPS | 16× | Serial | 16-lead TSSOP | 10.5 | 5.95 |
| AD7766-2 | 115.5 | 32 kSPS | 32× | Serial | 16-lead TSSOP | 8.5 | 5.95 |
| AD7767 | 109.5 | 128 kSPS | 8× | Serial | 16-lead TSSOP | 15 | 8.50 |
| AD7767-1 | 112.5 | 64 kSPS | 16× | Serial | 16-lead TSSOP | 10.5 | 8.50 |
| AD7767-2 | 115.5 | 32 kSPS | 32× | Serial | 16-lead TSSOP | 8.5 | 8.50 |

**FREE OFFER**
Samples and Data Sheets

**www.analog.com/V8ADC**

# IF Diversity Chipset Eases Wireless Base Station Design Challenges

As the industry migrates from voice-centric services and embraces feature-rich, multimedia content, wireless infrastructure designers need devices that support the higher data bandwidths of next generation mobile communications platforms. To help address these needs, ADI has developed the industry's highest linearity digital VGA and the fastest IF diversity receiver, which, when combined, reduce the number of devices and enable complex multicarrier wideband digital receivers into mainstream production. This combination of best-in-class performance, power consumption, size, and cost is ideally suited to meet the wider bandwidth and multicarrier signal processing demands of today's wireless infrastructure equipment.

The AD8376 and AD6655 is the first dual-channel, digital VGA and IF diversity receiver combination optimized for 2.5G and 3G wireless base stations. This combination supports standards such as CDMA2000, UMTS, and TD-SCDMA, as well as WiMAX wireless equipment. These devices simplify system complexity and cost by handling both main and diversity channels in a simple device pair.

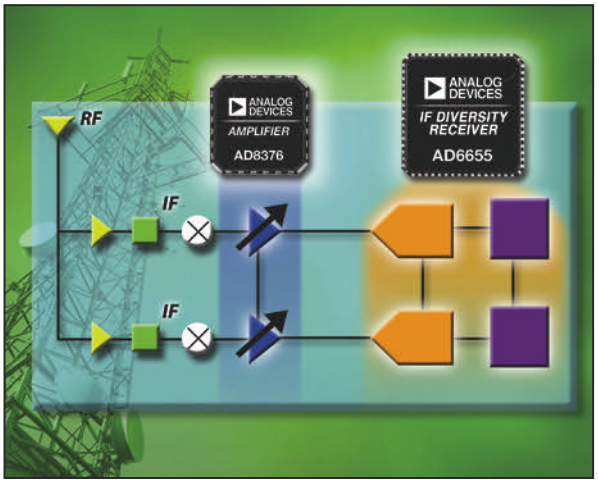
### *AD8375/AD8376 Digital VGA Features*

- OIP3: 46 dBm @ 100 MHz
- +44 dBm output IP3
- Bandwidth: 600 MHz
- Fine gain control range: 24 dB

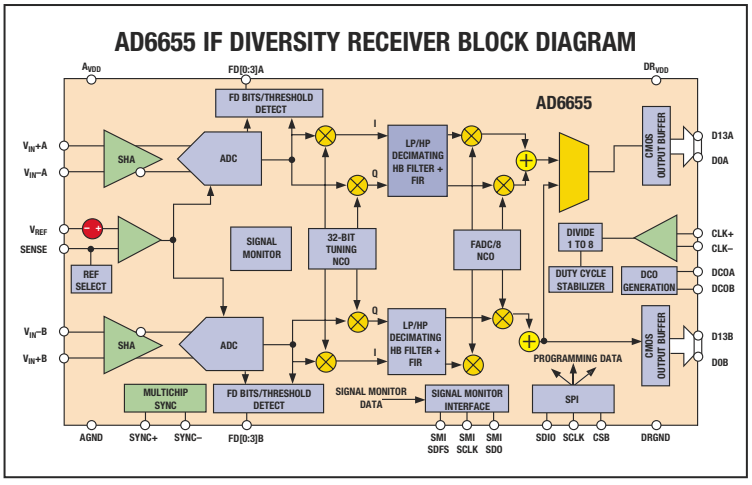
Technical seminar available on demand: "Options and Solutions for RF System Design" at *www.analog.com/onlineseminars*.

### *AD6655 IF Diversity Receiver Features*

- 14-/12-bit, 80 MSPS to 150 MSPS, dual ADC processing
- Digital downconverter with 32-bit NCO
- Decimating half-band filter
- Band-pass filtering function with FIR
- Signal monitoring and level detection
- 1 to 8 clock divider
- Multichip sync support
- Pin-compatible to AD9640, AD9627, AD9600




## AD6655 IF DIVERSITY RECEIVER BLOCK DIAGRAM



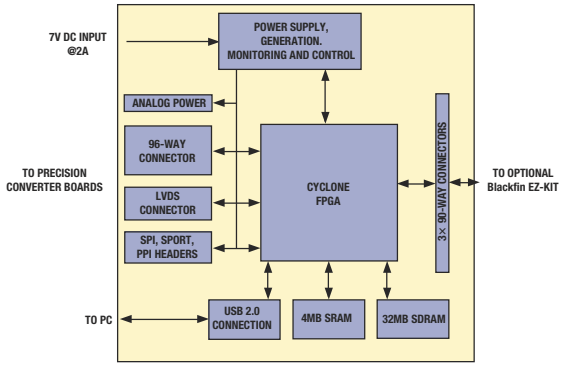

| Part Number | Description | Price ($U.S.) |
|---|---|---|
| AD6655-150 | 14-bit, 150 MSPS, IF diversity receiver | 93.50 |
| AD6655-125 | 14-bit, 125 MSPS, IF diversity receiver | 77.60 |
| AD6655-105 | 14-bit, 105 MSPS, IF diversity receiver | 64.60 |
| AD6655-80 | 14-bit, 80 MSPS, IF diversity receiver | 47.50 |
| AD6653-150 | 12-bit, 150 MSPS, IF diversity receiver | 57.97 |
| AD6653-125 | 14-bit, 125 MSPS, IF diversity receiver | 51.25 |
| AD8375 | Single-channel, digital IF VGA | 4.25 |
| AD8376 | Dual-channel, digital IF VGA | 6.25 |

**For samples and data sheets, visit www.analog.com/V8ADC**

## New Platform for Precision Converter Evaluation and Development Brings Efficiency to Product Selection and Design, Improving Time to Market

The next generation converter evaluation and development (CED) platform is intended for use in evaluation, demonstration, and development of systems using precision converters from ADI. It provides a thorough evaluation of converter performance and functionality as well as a development environment for integration of the converter into the end-user system.

For evaluation, the platform provides all the necessary hardware and software for direct and easy communication between the converter and the PC that transmits or receives data over a USB link. This functionality allows the converter to be controlled and programmed and enables streaming of data from the converter to the PC display. The software platform also provides a suite of analysis routines to allow evaluation of converter performance.




The CED system includes: CED board, USB A to MiniB cable, and a 7V to 15W power supply. It is priced at $500. The products that are currently supported are: AD7621, AD7641, AD7622, AD7643, AD7623, AD7766, AD7767, AD7356, AD7357, AD7262, and AD7264.

From a development viewpoint, the reconfigurable FPGA-based architecture of the board allows the FPGA to be reprogrammed at any time via the USB connection. This option allows the user to develop and run customized code to accomplish a design task. Standard Altera® FPGA tools are used, and the sample Verilog code is freely available to the customer so no software package purchase is necessary.

ADI provides LabVIEW™ code for standard converter functionality, and, for the first time, both ac and dc specifications will be available. Sections of this LabVIEW code will be available for customization by users. In addition, ADI is generating DSP code for the Blackfin® processor and will be making these software drivers available soon. Now, design engineers can gather data from a converter connected to the Blackfin processor—without the worry of configuring the Blackfin parameters to match the interface of the converter.

The CED board provides many interfacing options—SPI, SPORT, parallel, LVDS—that accommodate connection to a wide range of precision converter evaluation boards in different form factors. The CED also provides eight separate power supplies for external connection. For developments that require a processor as well as an FPGA, the CED board connects directly to a Blackfin processor EZ-KIT. For more information, visit *www.analog.com/EVAL-CED*.

## Next Generation Radio Frequency Transceivers Integrate Smart System Features

The AD9354/AD9355 family of WiMAX transceivers offers complete RF and mixed-signal system on a chip solutions. The transceiver integrates two high sensitivity direct-conversion receivers and channel-select filtering at baseband, eliminating the need for external SAW filters. The highly linear transmitter offers state-of-the-art EVM and spurious performance. A low phase noise LO path is achieved by an integrated fractional-N synthesizer. To enable low system cost, an on-chip crystal oscillator replaces the expensive external voltage controlled, temperature-compensated crystal oscillator (VCTCXO) with a simple 40 MHz crystal.

Additionally, the AD9354/AD9355 transceivers integrate smart system features such as self-calibration, automatic gain control, transmit power control, support for automatic frequency control, and auxiliary ADCs and DACs for system monitoring. This integration reduces the level of real-time signaling between the modem and the transceiver, dramatically simplifying the RF driver development and support. Additionally, the highly accurate closed-loop power control enables one-point factory calibration of transmit power. In contrast, competing transceivers require eight to 10 calibration points—increasing final test costs and extending development times.

| Part Number | Frequency Range (GHz) | Type (Rx/Tx) | Bandwidth (MHz) | NF (dB) | Tx EVM (dB) | Tx Gain Range (dB) | Digital Interface | Package Size LFCSP (mm) | Price ($U.S.) |
|---|---|---|---|---|---|---|---|---|---|
| AD9352 | 2.3 to 2.7 | 1 × 1 | 3.5 < BW < 20 | 3.7 | –38 | 0 to 58 | ADI/Q | 9 × 9 | 14.95 |
| AD9353 | 3.3 to 3.8 | 1 × 1 | 3.5 < BW < 20 | 3.7 | –38 | 0 to 58 | ADI/Q | 9 × 9 | 14.95 |
| AD9352-5 | 4.9 to 5.9 | 1 × 1 | 3.5 < BW < 20 | 5 | –33 | 0 to 58 | ADI/Q | 9 × 9 | 14.95 |
| AD9354 | 2.3 to 2.7 | 2 × 1 | 3.5 < BW < 10 | 3 | –38 | 0 to 58 | JESD207 | 8 × 8 | 11.45 |
| AD9355 | 3.3 to 3.8 | 2 × 1 | 3.5 < BW < 10 | 3 | –38 | 0 to 58 | JESD207 | 8 × 8 | 11.45 |

## Dual ADCs Deliver High Performance and Simplify AGC Input Function

In many communications receivers, the incoming signal strength varies widely. Automatic gain control (AGC) is used to maintain a fixed input signal level relative to an ADC to ensure that it meets the dynamic range requirements of the system. ADI's new ADC family simplifies this function with improved SNR, SFDR, and an integrated signal monitor.

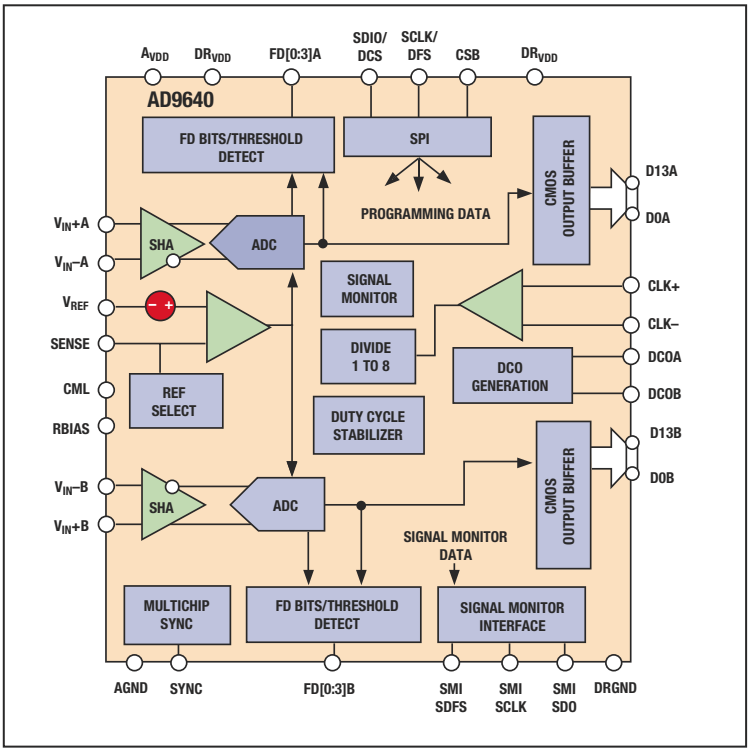
A high signal-to-noise ratio reduces the gain requirement for the AGC loop because the ADC can resolve smaller signals and operate with reduced input levels. The AD9640, a dual 14-bit ADC, delivers excellent SNR of 72.6 dBFS at 150 MSPS. In a similar manner, large interfering signals can cause the ADC to generate spurious components or harmonics. ADCs with higher SFDR performance allow the system to tolerate larger interferers without having to adjust the AGC. The AD9640 sets the industry benchmark for SFDR performance by delivering 84 dBc with a 70 MHz input at 150 MSPS. The AD9640 includes an on-chip signal monitor to measure the power of the input signal. This signal monitor block can be programmed via the serial port interface (SPI) to measure the complex power of both channels, the rms magnitude or peak level of each channel, and can correct for dc offset. Upper and lower thresholds are set by the user, and data can be read back through the SPORT or through four dedicated output pins.

The AD9640 is available in a 9 mm × 9 mm, 64-lead LFCSP and is optimized for low power with high performance. This new family of ADCs from ADI supports IF sampling of frequencies up to 450 MHz, an internal voltage reference, an on-chip clock divider and clock duty stabilizer, and flexible output configurations that support CMOS or LVDS interfaces. Recommended complementary ADI products to the AD9640 include the ADA4937-2, ADA4938-2, and AD8138 low distortion differential ADC drivers.

### Three options for easily evaluating AD9640 performance:

1. Model performance with a sine wave or two-tone input signal using ADI*sim*ADC. The ADC model and modeling engine are available at *www.analog.com/adisimadc*.
2. Model performance using a more complex waveform using VisualAnalog at *www.analog.com/visualanalog*.
3. Evaluation boards are available from *www.analog.com*. The AD9640 evaluation board interfaces with ADI's new FPGA-based data capture card, HSC-ADC-EVALCZ.

Technical seminar available on demand: "Design Considerations for Multichannel ADCs" at *www.analog.com/onlineseminars*.



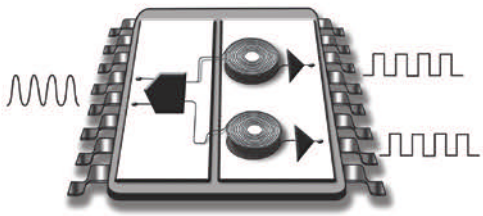

### IF Sampling Dual ADCs

| Part Number | Resolution (Bits) | Sample Rates (MSPS) | SNR (dBFS) | SFDR (dBc) | Power (mW) | Price ($U.S.) |
|---|---|---|---|---|---|---|
| AD9640 | 14 | 80, 105, 125, 150 | 72.6 | 84 | 452 to 820 | 37.50 |
| AD9627 | 12 | 80, 105, 125, 150 | 70.2 | 84 | 452 to 820 | 25.05 |
| AD9627-11 | 11 | 105, 150 | 66.7 | 84 | 600 to 820 | 24.65 |
| AD9600 | 10 | 105, 125, 150 | 61.6 | 81 | 600 to 820 | 11.26 |

# ADI Enables Motor Control Circuit Designers to Achieve Safer and More Efficient Control

Torque loop current monitoring must be tolerant of high voltages with respect to each phase as well as the controlling circuitry. Regulated safety standards from UL, CSA, and VDE require up to 3.75 kV of reinforced isolation.

The AD7400 and AD7401 isolated Σ-Δ ADCs provide the ideal solution for current monitoring in motor control applications. The integration of ADI *i*Coupler® digital isolation technology allows for 3.75 kV isolated high speed data rates with low power, which enables a more efficient control solution. Both of the devices, the AD7400 with its internal clock and the AD7401 with its external clock, use a 16-lead SOIC package and operate from a 5 V supply. The devices accept a ±200 mV signal range—making them suitable for a direct connection to current shunts. Both of the devices are housed in a 16-lead SOIC.



*i*Coupler digital isolation technology integrates chip scale transformer technology with an analog front end.

**APPLICATIONS**

- AC motor controls
- Data acquisition systems
- ADC + optoisolator replacements

| | |
|---|---|
| AD7400 | $4.00 |
| AD7401 | $4.00 |

*AD7400 and AD7401 Features*

- AD7400: 10 MHz data rate (internal clock)
- AD7401: 18 MHz date rate (external clock)
- Second-order modulator
- 16 bits and no missing codes
- ±2 LSB INL typical at 16 bits
- ±2 LSB INL typical at 16 bits
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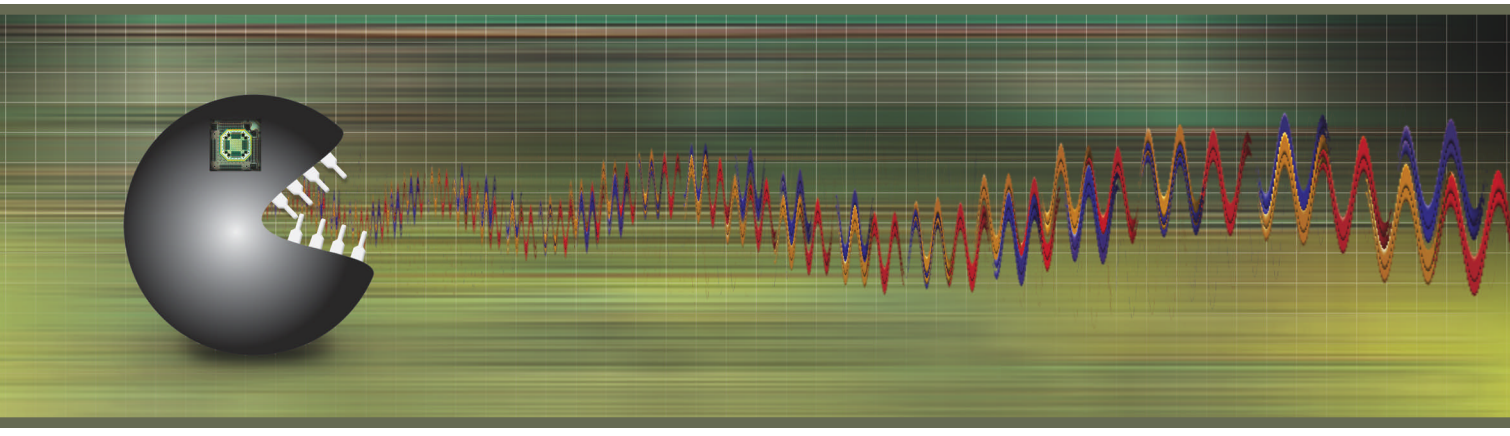


COMPLEX ICs ARE NOT ONLY ABSORBING MORE OF THE SYSTEMS AROUND THEM, BUT ALSO SWALLOWING THE TEST EQUIPMENT DESIGNERS USE TO BRING UP, EVALUATE, AND CALIBRATE THE CHIPS.

# AS SOCs GROW, TEST-AND-MEASUREMENT INSTRUMENTS MOVE ON-CHIP

BY RON WILSON • EXECUTIVE EDITOR

It's just geometry. As system-level ICs grow larger and more complex, they become impossible to observe and stimulate. Internal nodes aren't accessible to bonding pads or even to probes. Signal voltages are small, noise thresholds are tiny, and drive strengths are negligible. As critical circuits reach gigahertz frequencies, it becomes physically impossible to get an accurate representation of signals off the die, even if you can probe the circuit.

Yet the need remains. Chip designers must be able to observe and stimulate individual blocks in an SOC (system on chip) to bring up the silicon. Manufacturing-test engineers must be able to create fast test programs on affordable test equipment. Increasingly, chip designers must also create autocalibration routines that can compensate critical circuits for process, voltage, temperature, impedance, and noise variations while the chip is in use. The only apparent option is to move test-and-measurement instruments—the racks of logic analyzers, bus analyzers, communications testers, and oscilloscopes that populate the bring-up lab—onto the chip itself.

And this option is now available. Beginning perhaps with debugging facilities built into CPU cores, extending through bus diagnostic blocks and logic built-in self-test blocks, on-chip instrumentation is today extending into high-speed transceivers and RF circuits. In the future, you may see on-chip analog instrumentation for characterization and calibration routinely becoming part of analog design (see **sidebar** "MEMS accelerometers need instrumentation, too").

## BEGINNING IN THE CPU

The idea of building debugging hardware into a CPU dates back at least to the IBM 360 architecture. But the race to fit more complex CPU cores into less die area meant the concept became lost in the early days of SOC design. It resurfaced because of necessity.

"As processor complexity and frequency increased, it became just too difficult to control the core through external circuitry," says William Orme, general manager of the CoreInsight debugging program at ARM. "Designers resisted adding to the core area for debug, but it became a trade-off of die area versus pain. Eventually, in-core debug became cost-effective in the overall cost of the SOC. Then, it simply became obligatory."

During that evolution, the basic techniques have not changed. Designers still need to put the CPU core in a known state, start it running, observe and record the resulting sequence of states, and stop the core again when something interesting happens. Hardware integrated into the core can accomplish all these things with essentially no impact on performance or energy consumption during normal operation.

But as SOCs evolved, the CPU core ceased to be the only problem. The growing web of buses—wide, fast, seg-

mented, and multilayer—that spread out from the CPU also became unobservable. So, ARM and other vendors of interconnect IP (intellectual property) built debugging circuitry into the interconnect architecture, just as they had built it into the CPU.

"In an AHB [advanced-high-speed-bus] multilevel interconnect, designers need to monitor what is going on at any level of the interconnect: the source, destination, and content of every transaction," Orme says. "That [process] requires monitoring from inside the die."

The situation grows even more complex as SOCs evolve from a single CPU core at the center of a bus network to multicore designs in which numerous processing sites are active at once. Now, an event may be not simply the state of a core or a bus but a complicated merging of state sequences from a number of processors and interconnect structures in different clock and voltage domains. Just being able to start and stop such a system and to capture some idea of its actual state becomes a challenging problem, Orme admits.

**AT A GLANCE**

- Chip designers are starting to design test-and-measurement instruments into their complex ICs.
- The movement toward designing instruments into ICs started with digital debugging hardware for CPU cores and buses.
- Now, designers are also building analysis instruments into high-speed-I/O blocks.
- Designers are integrating more complex analog and RF instruments into the inner workings of high-frequency chips, such as read-channel ICs.

The growing complexity may be shifting the emphasis in on-chip-debugging circuitry away from the CPU core and toward a more system-level approach. ARM, for instance, offers a cross-triggering switch matrix that attempts to bring together state signals from different blocks in the SOC. And processor-independent debugging-hardware companies, such as Dafca, are also emerging.

"Design teams have been trying to create a comprehensive debug strategy by combining CPU-debug facilities with their own in-house-designed on-chip instrumentation," says Paul Bradley, Dafca's vice president of engineering. "But as the complexity of the SOC grows, voltage and clock domains proliferate,

## MEMS ACCELEROMETERS NEED INSTRUMENTATION, TOO

**MEMS (microelectromechanical-system) accelerometers, with their accuracy, low power, and low cost, are revolutionizing a number of applications. Fuses for automotive air bags, attitude and motion sensors for computer-input devices, and sensors for automotive attitude-control systems are some large-volume examples.**

**The acceleration-sensing elements are often differential capacitors in which silicon springs suspend one plate of the capacitor above the other two. Acceleration causes the suspended plate to shift, changing the relative capacitance of the two capacitors and, hence, the relative amplitude of signals passing through them. Properly designed and fabricated examples of such structures are sensitive, accurate, and durable. But they require calibration. Changes in applied voltage and ambient temperature can change the sensitivity of the device, and each sensor has an offset reading at 0g that the user must measure.**

**In high-volume applications, that requirement is not a problem, according to Bob Scannell, business-development manager at Analog Devices. If you use hundreds of thousands or millions of sensors, it's no great cost to set up a calibration tool that connects to the sensors and spins them at known rates in a temperature chamber. But, in lower volume applications in the industrial world, it makes great sense to have on-chip instrumentation to calibrate the devices ahead of time (Figure A). "Precalibration removes barriers to use," Scannell says.**

**By embedding a temperature sensor and a microcontroller in the MEMS device, for instance, the vendor can preload temperature-compensation tables and have the chip remove temperature-based variations on the fly. Similarly, firmware can take the chip through an autozeroing procedure to establish a reference horizontal plane in-system, electrically stimulate the MEMS structure, and compare the output with a known reference for a quick pass/fail-operation test.**

**In examples such as these, on-chip instrumentation is worth the silicon investment not because there is no other way to make the measurements or even to reduce exorbitant test cost, but simply to make the device easier to use, opening new markets.**

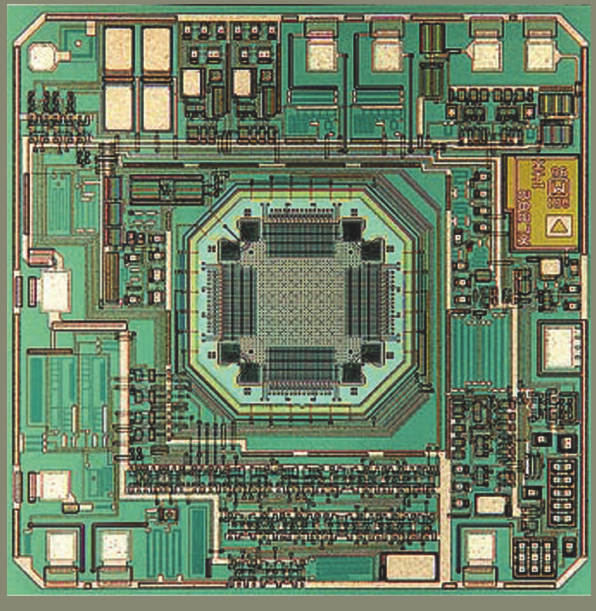
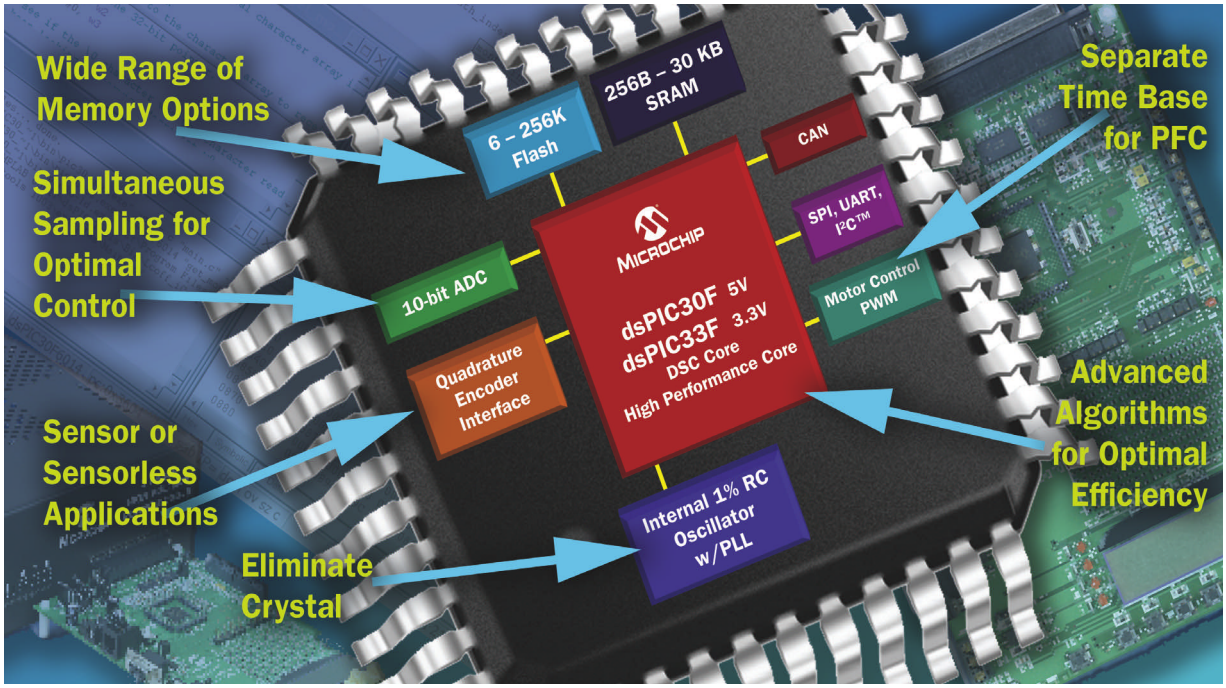


Figure A MEMS accelerometers, such as Analog Devices' ADxl202, require significant on-chip instrumentation for bring-up, test, and in-circuit calibration.

# More Efficient 3-Phase Motor Control

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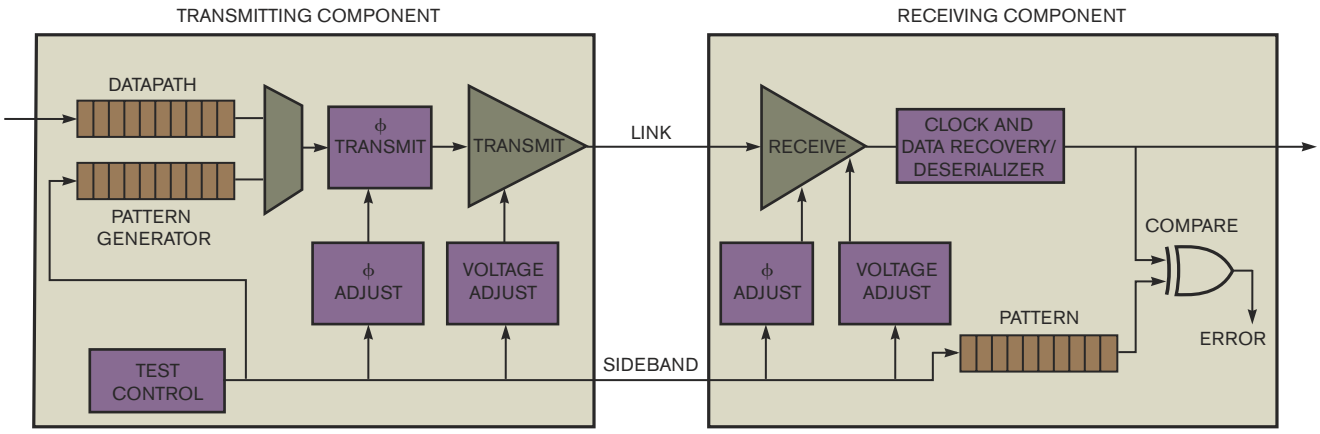


Figure 1 On-chip instruments permit a variety of test-and-measurement procedures in this Rambus serial-link architecture.

and reuse gets more important, designers need a comprehensive approach, not a collection of ad hoc designs."

Dafca Chief Executive Officer Peter Levin adds another dimension to the concern: "As this complexity grows, so does the complexity of the debug software you need to control the hardware and make sense of the data. Today, the debug-software effort is at least 10 times greater than the effort to design and integrate the debug hardware." Again, reuse is vital, and licensing the whole thing from a specialist looks more and more reasonable.

Dafca's architecture gives an idea of how complex full-chip debugging support has become. Dafca works with, rather than replaces, the debugging hardware in the design's CPU or DSP cores. But it adds "analysis instruments"—elaborate but compact reprogrammable state machines that can stimulate a block by pre-empting the block's inputs for some number of cycles, monitor outputs of a block, and report exceptions into a global network.

"Deployment of the instruments is very application-specific," Bradley says. "Usually, a design team will use two to six analysis instruments on a chip, often associating one with each major design domain. In this way, they can observe key interfaces and control points—usually at the second level in the design hierarchy." Pulling together the information from the instruments and the processor cores into a cohesive picture of the operating chip and providing a level of abstraction at which designers can define and impose a chipwide state are critical needs in any such architecture. That requirement may explain the huge software component of the design.

Digital on-chip instrumentation, then, has evolved from fairly simple debugging cores within CPU cores to much more sophisticated hardware/software systems that designers base on distributed state machines and a triggering-and-control network on the chip. As SOCs become still more complex, the next step seems to be full logic-analysis capability on the die, with programmable triggers, large trace and vector buffers, and an ability to probe nodes within the chip.

## THE ANALOG DOMAIN

Analogous to the trend in on-chip digital instrumentation, there is growing interest in generating and measuring analog signals with on-chip instruments. And if it's fair to trace the origins of digital instrumentation to CPU cores, the analog instruments are starting out in the cores of high-speed serial interfaces. But the techniques are branching out in the analog domain, as well, incorporating sensor-based measuring systems for autocalibration, mixed-signal servo systems, and instruments for validation and test.

As in the digital world, the driving force behind on-chip instrumentation of high-speed I/O is the growing invisibility of key signals. "The mere existence of an external probe alters a high-speed link," says Rich Perego, senior principal engineer at Rambus. "Yet, there is value in being able to look at a waveform."

"Often, you can probe the transmitter directly," adds Ken Chang, design-engi-

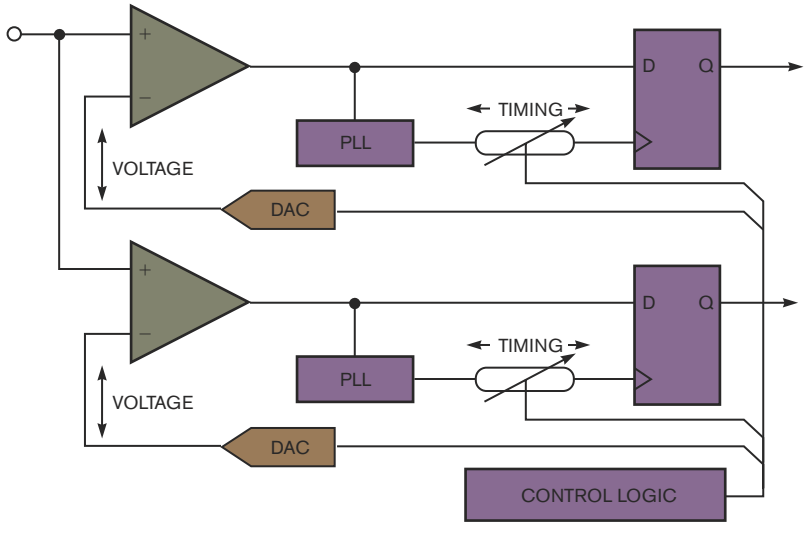


Figure 2 Vitesse has recently taken receiver instrumentation a step further, devising an interesting two-channel approach.


# SIMULATION SOFTWARE
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neering manager at Rambus. "But you can't just probe the receiver. You have to look at the receiver indirectly by extracting data on-chip and inferring eye diagrams or bathtub diagrams."

This approach has become increasingly important in high-speed receivers, in which it is otherwise impossible to see what is going on inside the block. You can't see from the outside what the signal looks like just before or just after equalization, according to Eric Sweetman, senior applications engineer at Vitesse. You have to make those observations from inside the receiver.

Rambus approaches this problem by using the receiver as, in effect, its own measuring instrument. The process starts with integrating programmable pseudorandom-pattern generators and bit-stream comparators into the I/O blocks. Designers can then add enough circuitry to digitally adjust the transmitter and receiver (**Figure 1**). In the case of the transmitter, for instance, this method means putting digital inputs and DACs on controls for the current swing and phase and being able to modify the equalization-tap coefficients. "That [approach] allows us to create shmoo plots of transmitter performance by sweeping timing and voltage," Perego explains.

In the case of a receiver, it might mean adjusting the receiving amplifier's phase and gain. That process allows designers to extract timing margins, for instance, by sweeping phase and watching the bit-error-rate accumulator on the output of the bit-stream compare block.

The art of such instrumentation is to do as much as possible in the digital domain. You can digitally control receiver phase by manipulating the digital-feedback path in a delay-locked loop, for instance. Or you can adjust gain by providing a digital value to a small DAC, which in turn adds an offset to a critical node. These insertions into the circuitry are not trivial, particularly in the case of analog nodes, in which any change has the potential to break a circuit. But they are achievable.

Vitesse has recently taken receiver instrumentation a step further, devising an interesting two-channel approach (**Figure 2**). This idea sets one channel—usually the receiver's primary data channel—at the center of the eye. Designers can then sweep a second, essentially identical channel across the space

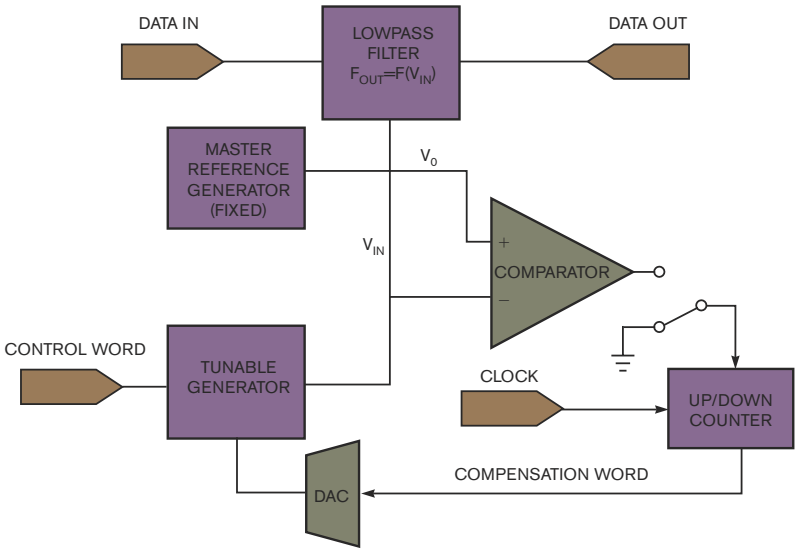


Figure 3 A simple comparator-based loop can remove drift from the voltage source that determines a filter cutoff frequency (courtesy STMicroelectronics).

of phase and amplitude points by altering the receiver's phase and gain, stopping at each point, accumulating enough data to accurately estimate the bit-error rate, and moving on. The result after software postprocessing is either an eye diagram or a bathtub plot of data that the receiver itself collects. Because the second path is physically identical to the read path that is taking the measurements, the data are more accurate than a probe and scope could ever achieve, Sweetman says. The designer can see the exact signal that's going into the receiver's sampler from the equalizer, not a distorted approximation.

**THE ART OF SUCH INSTRUMENTATION IS TO DO AS MUCH AS POSSIBLE IN THE DIGITAL DOMAIN.**

High-speed I/O is not the only application for such ideas, however. STMicroelectronics, for example, puts considerable instrumentation into its high-end disk-read-channel ICs. Again, the emphasis is on using the circuitry as much as possible to perform measurements under external control. But, in this case, the added circuitry can be complex.

Angelo Dati, architecture manager for the data-storage division at STMicroelectronics, says that the internal instruments within a read-channel chip assist with initial troubleshooting and calibration of the chip; help characterize the complete media/electronics system once the chip is installed; and provide continuous compensation for voltage, temperature, head-height, and other variables during operation.

Accordingly, the read channel has a variety of measuring instruments. Simple sensors for temperature and voltage, for instance, run to comparators and linear filters, which the controlling processor can interrogate to determine whether to launch a calibration procedure on a local finite-state machine. The state machine runs a closed-loop calibration procedure in which it can alter voltage offsets, gains, and bias points to correct problems, such as the tendency for the channel's lowpass-filter-cutoff point to drift with temperature.

More sophisticated measurements not only compensate for variations during operation, but also help designers and production engineers tune the chip to a particular head/media combination. One of these measurements sees use in

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# Intersil USB Switches

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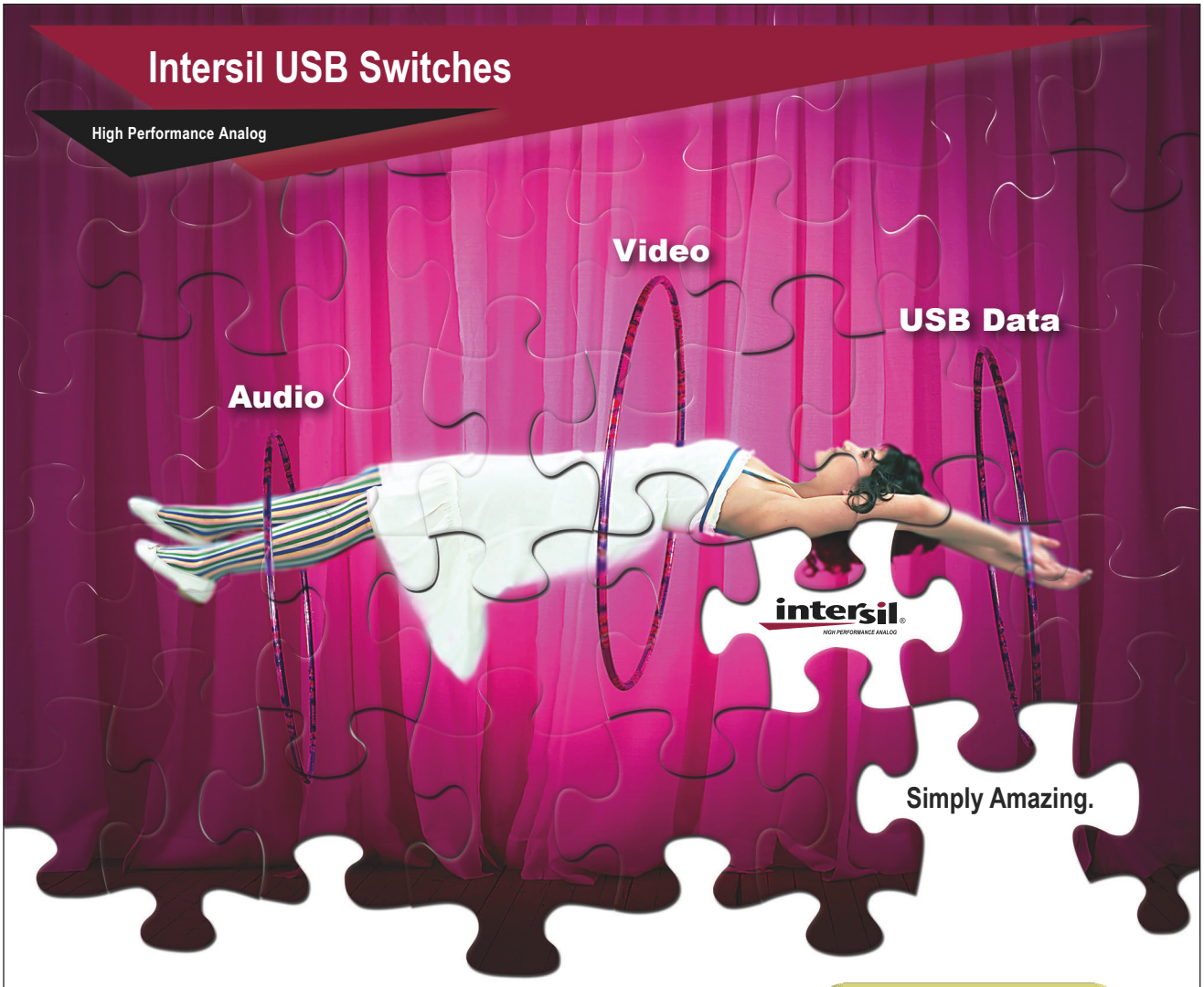
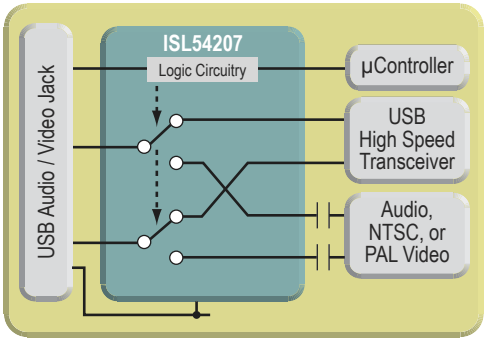
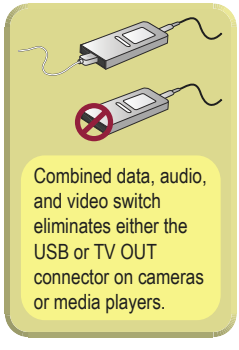



Intersil's tiny USB Switch **enables charging, audio, video, and high speed data through a single connector.**

Combined data, audio, and video switch eliminates either the USB or TV OUT connector on cameras or media players.

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| Device | Audio THD 32Ω (%) | USB Speed | Video Diff Gain Phase |
|---|---|---|---|
| ISL54207 | 0.06 | 480 | 0.28 / 0.04 |
| ISL54208 | 0.06 | 480 | 0.28 / 0.04 |
| ISL54415 | 0.007 | 12 | 0.04 / 0.03 |
| ISL54416 | 0.007 | 12 | 0.04 / 0.03 |
| ISL54417 | 0.007 | 12 | 0.04 / 0.03 |

**Audio / Data**

| Device | Audio THD 32Ω (%) | USB Speed |
|---|---|---|
| ISL54205A | 0.06 | 480 |
| ISL54206 | 0.06 | 480 |
| ISL54400 | 0.007 | 12 |
| ISL54401 | 0.007 | 12 |
| ISL54402 | 0.007 | 12 |

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an adaptive-loop system based on pattern matching, Dati says. Instrumentation within the chip generates an analog waveform that the system feeds into the read circuitry and compares with the incoming signal from the read head, giving a frequency-error signal. This signal provides feedback for adapting to the noise and nonlinearity characteristics of the head/media combination. The process is closed-loop. But, Dati says, "There is no proof of convergence. We have to seed the adaptive loop with a good starting value for it to work."

Still another analysis is useful in silicon bring-up and in manufacturing for performing harmonic analysis on the drive assembly. The chip actually contains what Dati describes as "a coarse spectrum analyzer—like an FFT engine but simplified to look for some specific frequencies, so it is simpler than a general-purpose spectrum analyzer." The instrument's harmonic analysis has a number of valuable purposes. By looking for specific frequencies that shouldn't be there, for instance, you can detect and measure nonlinearity in the head/media subsystem. And, by looking at the frequency envelope, you can estimate the magnetic spacing—the height of the head above the media. "With today's drives, you have to do that," Dati explains, "because if you don't measure and adjust the head height, ordinary differences in atmospheric pressure could cause a head crash."

A spectrum analyzer might seem like a large instrument to tuck inconspicuously into a highly cost-sensitive chip. But in reality, "receivers are getting so big that it's easy to hide some instrumentation circuitry in the design," Dati says.

That observation may be a good introduction to the future of on-chip instrumentation. As chips get more complex, there will be not only greater need for instruments on the die, but also more opportunities to exploit the functional circuitry to quickly move analog measurements into the digital domain. And there will be more space in which to stash even a fairly complex block, such as a modified FFT engine.

The next step is probably to follow what has been happening on the digital side: Pull together analog measurements from both the time and the frequency domains from different portions of the chip to provide a picture of the full state of the mixed-signal system. Only with such on-chip tools may it prove possible to debug the next generation of complex chips and to keep the generation after that running at all. EDN

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# TIGHTENED POWER-EFFICIENCY REGULATIONS FORCE POWER SUPPLIES TO KEEP UP

BOTH VOLUNTARY AND MANDATORY POWER-REGULATION STANDARDS HAVE FORCED MANUFACTURERS TO MEET MINIMUM POWER-EFFICIENCY STANDARDS OR RISK LOSING CUSTOMERS—AND, SOMETIMES, MARKETS. NEW VERSIONS OF STANDARDS AND NEW MANDATORY FEDERAL REGULATIONS CALL FOR HIGHER EFFICIENCIES. THESE REGULATIONS MAKE MORE SOPHISTICATED CONVERTER TOPOLOGIES REASONABLE APPROACHES—EVEN FOR THE LOWLY WALL WART.

BY MARGERY CONNER • TECHNICAL EDITOR

# ENERGY STAR,

## A JOINT EFFORT BY THE US ENVIRONMENTAL PROTECTION AGENCY AND THE US DEPARTMENT OF ENERGY, PROVIDES A VOLUNTARY-COMPLIANCE PROGRAM TO IDENTIFY AND PROMOTE ENERGY-EFFICIENT PRODUCTS TO REDUCE GREENHOUSE-GAS EMISSIONS.

Until recently, external power supplies for consumer devices such as cordless phones and laptop computers were notorious power hogs. Consumers generally considered any adapter, or "wall wart," that provided enough power at the correct voltage and current for the cheapest price was good enough. With efficiency levels as low as 40 to 50%, these adapters wasted power as low as 1W each—too low to get an individual consumer's attention. However, multiply these adapters by the millions that exist in the United States alone, and you've wasted enough power to require extra power stations. The Energy Star program, which has since 1992 been offering voluntary-compliance standards for household appliances, has now created a similar specification for EPS (external-power-supply) products.

Energy Star, a joint effort by the US Environmental Protection Agency and the US Department of Energy, provides a voluntary-compliance program to identify and promote energy-efficient products to reduce greenhouse-gas emissions (**Figure 1**). The first Energy Star specification covered relatively large appliances, such as computer monitors and refrigerators. In 2005, Energy Star proposed a version for EPS devices (**Reference 1**). According to Andrew Smith, product-marketing manager for Power Integrations, Energy Star has become such a powerful brand that companies follow it as if it were mandatory. In addition, it serves as the basic specification for other countries' and states' regulations.

The success of any of Energy Star's voluntary programs relies on consumers' desires to choose an environmentally responsible electronic device and to save on energy bills, which may offset any increase in the electronic equipment's price. The CEC (California Energy Commission), taking a less sanguine view of consumers' eagerness to embrace environmental responsibility, made mandatory what were essentially Energy Star's voluntary regulations for electronic equipment sold in California. The CEC mandatory regulation went into effect on July 1, 2007. After some equipment manufacturers' initial whining, compliance began and effectively set the standard for all equipment sold in the United States; California accounts for approximately 10% of the national economy.

However, power-supply manufacturers have expressed concern that other states could follow California's lead, creating a mare's nest of conflicting regulations. With the passage last December of the Energy Independence and Security Act of 2007, the US government has established a minimum level of efficiency for EPS devices corresponding to the levels that the CEC set. The new act supersedes any mandatory state regulations (**Table 1**). The effective date is the same as that for CEC's new, more stringent regulations: July 2008.

The federal levels are just the minimum compliance levels that EPS devices need to meet for government, corporate, and individual buyers. Energy Star is still important, even as the US government begins mandating efficiency levels because the organization keeps up with improvements in technology that enable cost-effective increases in efficiency. Energy Star 1.1 for external adapters is not onerous in its efficiency standards. For example, a 36W ac/dc adapter must meet 80% minimum average efficiency in active mode. Its maximum no-load power draw is 0.75W (**Table 2**). However, Energy Star has published a draft of EPS Version 2.0 with tighter regulations (**Reference 2**). That 36W power supply must now meet an average minimum of 87% in active mode, which is a decrease in dissipated power of one-third; the standby power drops to 0.5W or less. Energy Star's pragmatic approach to moving the electronics sector toward efficiency was targeting the "low-hanging fruit" in the initial version: selecting

### AT A GLANCE

- The Energy Independence and Security Act of 2007 establishes mandatory efficiency levels for external power supplies. These directives supersede any mandatory regulations at the state level.
- Manufacturers could comply with the voluntary first version of Energy Star by using more efficient components. The second round will require more efficient and more complex power-supply designs.
- Energy Star's second version appears to be setting an international de facto standard.

more efficient components and relatively simple fixed-frequency switching topologies, using more copper in the transformer, and paying a premium for low-on-resistance MOSFET switches. Energy Star then in subsequent versions moved the industry toward designing increasingly efficient and complex power supplies.

The authors of the Energy Star 2.0 draft composed it after reviewing the EPS test data from a worldwide test database of 1800 EPS devices. The agency is reviewing comments from stake-holder companies; the revised Version 2.0 will go into effect in the second half of this year. Version 2 is notably more stringent than Version 1.1. For example, Version 1.1 lumped together ac/ac and ac/dc converters, dividing them only by "nameplate power"—the maximum power listed on the devices' enclosures. Version 2.0 separates them in all specifications, however. In addition, Version 2.0 stipulates an increase in minimum-active-mode-energy-efficiency requirements, a decrease in maximum-no-load-power limits, and the requirement for PFC (power-factor correction) in power supplies with a nameplate-power output of 75W or more (**Table 3**).

**TABLE 1 THE ENERGY INDEPENDENCE AND SECURITY ACT OF 2007 MANDATES**

| Active mode | |
|---|---|
| **Nameplate-output power ($P_{NO}$)** | **Required efficiency** (decimal equivalent of percentage) |
| <1W | $0.5\times P_{NO}$ |
| 1 to 51W | $[(0.09)\ln(P_{NO})]+0.5$ |
| >51W | 0.85 |
| **No-load mode** | |
| **Nameplate-output power ($P_{NO}$)** | **Maximum consumption** |
| <250W | 0.5W |

Version 2.0 requires as much as 87% average active-mode efficiency, up from 80% in Version 1.1. The increase of 7% for a 36W power supply may not sound like much, but when you compare it with the formerly allowable loss of 20%, that 7% amounts to reducing the loss by a third—a significant amount. Bob Mammano, chief power technologist and fellow at Texas Instruments, points to this difference as indicative of the jump in sophistication that Version 2.0-compatible designs require. "As the spec gets tighter, you don't reach it just by improving what you've been doing; you've got to actually do things differently—like change the topology to minimize switching losses by going to resonant switching and multistate operation—not just let it run at the high switching frequency that's best for full load when it's in standby." TI's UCC28600 PWM (pulse-width-modulated) controller is one of the first that the company designates as "green," incorporating frequency foldback and green-mode operation to reduce the operation frequency at light- and no-load operations. The chip costs 65 cents (100).

Vipin Bothra, application manager for STMicroelectronics, agrees that the most cost-effective way to increase EPS efficiency over a wide range of loads and conditions is to look toward a more complex controller IC. The company's L6668 controller works in three modes by sensing and responding to the output load. For example, you could set one mode to have 0 to 1W output power, the second mode to have 1 to 30W, and the third to have 30W to full power. The L6668 costs 68 cents (10,000).

## ENERGY STAR: ACCEPTABLE TO ALL?

**As recently as 2006, many in the electronics industry worried that all the US and international regulations on "green" power would result in expensive headaches for companies trying to sell into a global market. However, countries are aligning themselves behind Energy Star's programs, especially for EPS (external-power-supply) and battery-charger devices, providing a reason for cautious optimism. If an adapter meets Energy Star regulations, especially the proposed Version 2.0, that adapter will likely also meet international regulations. However, these regulations are in a state of flux for many reasons, not the least of which is that a country's "greenness" is a politically charged topic. You should be aware of these international organizations and monitor their new regulations.**

**Among those providing information on these topics, Power Integrations offers perhaps the best online aggregation of power-efficiency regulations (www.powerint.com/greenroom). A group of German government agencies and businesses operates another voluntary-labeling plan, Blue Angel (www.blauer-engel.de). The CEC (California Energy Commission) mandates that electronics equipment sold within California must meet its specifications, but its requirements are currently within Energy Star guidelines. However, this month, the CEC's Efficiency Committee conducted a workshop to seek comments from interested parties "regarding the scope of the next rulemaking to amend the Appliance Efficiency Regulations," including battery chargers, so follow the committee decisions for future specifications.**

**The CECP (China Energy Conservation Project, www.cecp.org.cn/englishhtml/index.asp) seeks voluntary compliance, and the European Code of Conduct (http://re.jrc.ec.europa.eu/energyefficiency/html/standby_initiative.htm) seeks voluntary compliance in the European Union. The Japanese Ministry of Economy, Trade and Industry (www.meti.go.jp/english) organized the Top Runner (www.eccj.or.jp/top_runner/index.html) voluntary label, which covers standby requirements for computers, copiers, TVs, and VCRs. The US Executive Order 13221 "1-Watt Standby" Order (http://oahu.lbl.gov) is a mandatory regulation for electronic products that federal agencies purchase as specified by the FEMP (Federal Energy Management Program).**

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**TABLE 2 ENERGY STAR 1.1 CRITERIA**

| Energy efficiency for active mode | |
|---|---|
| **Nameplate-output power ($P_{NO}$)** | **Minimum average efficiency in active mode** |
| 0 to 1W | $\geq 0.49 \times P_{NO}$ |
| >1 to 49W | $\geq [0.09 \times \ln(P_{NO}) + 0.49]$ |
| >49W | ≥0.84 |
| **Energy consumption for no-load mode** | |
| **Nameplate-output power ($P_{NO}$)** | **Maximum power in no load** |
| 0 to <10W | 0.5W or less |
| 10 to 250W | 0.75W or less |

The search for higher efficiency eventually reaches the point of diminishing returns. For example, Power Integrations' *Mr Green* blog relates the discussion of an Energy Star DTA (digital-television-adapter) meeting in 2006. A participant at the meeting presented a low-cost DTA design that included a circuit for a low-parts-count, cost-effective, energy-efficient, 5W ac/dc external adapter (**Reference 3**). The proposed adapter had an active-on-mode efficiency of 74%, outperforming the 63% minimum that Energy Star, the CEC, the European Union, Korea, and others then required (see **sidebar** "Energy Star: acceptable to all?"). This 74% was a major energy-efficiency improvement over the typical 50% linear-power-supply efficiency in active mode, and the adapter's BOM (bill-of-materials) cost was just a few cents more than the linear-transformer product. Pay-back time from energy savings for the consumer was just a few months. Improving the no-load efficiency by more than half—from 100 to 40 mW—was essentially free. However, going to the proposed 2.0 Energy Star level requires a more sophisticated controller IC; fortunately, these IC prices are dropping, making the higher efficiency attainable at a still-reasonable price.

Energy Star EPS 2.0's first inclusion of PFC specifies it for only those power supplies with a nameplate power of 75W or greater. A traditional power supply with a diode rectifier feeding a capacitor draws current only when the voltage at the load exceeds the voltage at the bulk capacitor. Because the rectifier is nonlinear, the input current is nonlinear, with energy appearing in high-order harmonics. The power supply takes this energy from the ac mains, even though it delivers only a fraction of it to the load—hence the term "power factor," which is the ratio of usable energy at the load to the energy that the power company provides. PFC circuitry is usually in the form of an active boost or buck converter.

Energy Star's requirement for PFC adds significant cost to many adapters because it mandates that manufacturers meet a new stipulation. For example, TI's 28060 PFC IC, which you can use with the 28600 converter, costs $1.75 (100). The intent of the Energy Star regulation is to prevent an inefficiency beyond just the power supply itself. The stated purpose of Energy Star is not just to increase the efficiency of each product, but also to reduce greenhouse-gas emissions. The better an application's PFC, the less power it loses in the power-transmission network and the lower the amount of greenhouse gases it emits.

The fact that the proposed Energy Star 2.0 doesn't cover PFC at power levels below 75W might lead you to believe that PFC is too unimportant to worry about at lower levels, but this assumption is wrong:


Figure 1 Although the Energy Star label on major appliances has a flashy Energy Star-compliance logo, the label on external power supplies is much smaller. Space constraints generally limit the designation to either III or IV, with III being the current spec, and IV indicating the tighter Version 2.0 proposed for 2008.

## HOW MUCH DOES ENERGY STAR SAVE?

**Demand for electricity in the United States is growing at twice the pace of new power-generation capability, a trend that could lead to supply problems in a couple of years (Reference A). Before deregulation in the 1990s, the federal government could simply have ordered utilities to build more power plants. Now, a strong reliance exists on market incentives to reduce consumer demand for energy. The US DOE (Department of Energy) and Environmental Protection Agency's Energy Star program comes in at this point. Much of the nation relies on market incentives, such as the ever-increasing price of energy from the grid, to encourage building resources or to prompt customers into reducing energy use. Energy Star allows products that meet its efficiency specifications to label themselves as such, appealing to cost-conscious consumers. In 2006 alone, according to the program's 2007 status report, the use of Energy Star-labeled equipment and appliances saved more than 1194 trillion BTU of energy and prevented carbon emissions of 21.1 million metric tons (Reference B). And the same report states that Energy Star labeling in external power supplies saved 2 trillion BTU, or $17 million.**

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**A Smith, Rebecca, "Electricity Demand Is Far Outpacing New-Supply Sources," *The Wall Street Journal*, Oct 17, 2007, pg A17, http://online.wsj.com/article/SB119258797074161584.html.**

**B Sanchez, Marla, Carrie A Webber, Richard E Brown, and Gregory K Homan, "Savings Estimates for the Energy Star Voluntary Labeling Program 2007 Status Report," Lawrence Berkeley National Laboratory, Environmental Energy Technologies Division, March 23, 2007, http://enduse.lbl.gov/info/LBNL-56380(2007).pdf.**

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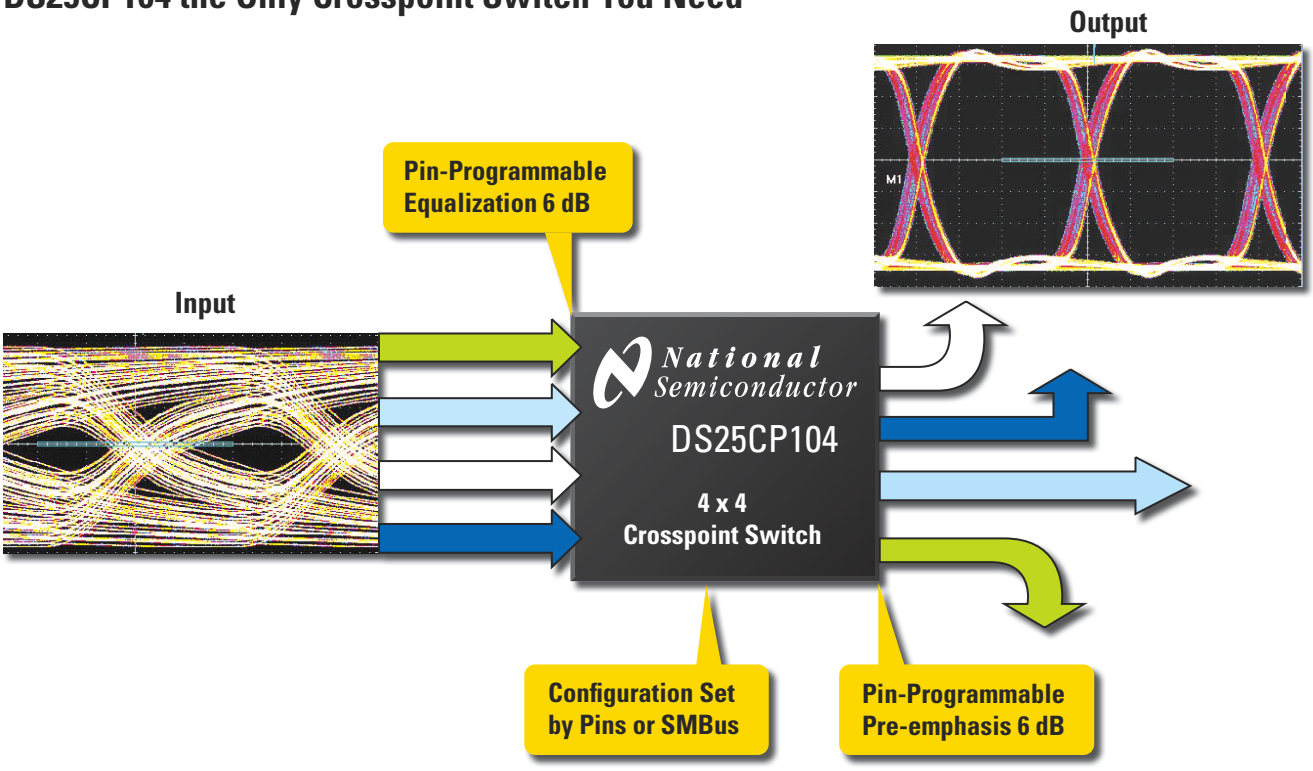


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**TABLE 3 PROPOSED ENERGY STAR VERSION 2.0 EFFICIENCY SPECS**

| Active mode | |
|---|---|
| Nameplate-output power ($P_{NO}$) | Minimum average efficiency in active mode (expressed as a decimal) |
| 0 to 1W | $\geq 0.44 \times P_{NO} + 0.145$ |
| 1 to 36W | $\geq [0.08 \times \ln(P_{NO})] + 0.585$ |
| >36W | ≥0.870 |

| No-load mode | | |
|---|---|---|
| Nameplate-output power ($P_{NO}$) | Maximum power in no load | |
| | AC/AC EPS | AC/DC EPS |
| 0 to <50W | 0.5W or less | 0.3W or less |
| 50 to 250W | 0.5W or less | 0.5W or less |

Power systems for lighting applications have for several years included PFC. EPS designers and vendors tend to consist of a fragmented group going after a fiercely competitive low-end market in which pennies make a significant difference in the profit margin. In addition, the end user is usually a consumer purchasing just one power supply; in this case, a small difference in efficiency makes no noticeable difference in the user's power bill. In the lighting industry, however, just five or six major players dominate, and the end application is often a significant installation in which even a few percentage points of increased power efficiency can result in noticeable energy-bill savings (see **sidebar** "How much does Energy Star save?"). STMicroelectronics' Bothra says that most of the company's PFC-control chips find use in lighting applications because PFC can make a difference at power levels of as low as 16W.

Energy Star has finalized its specification for solid-state lighting, with a possible implementation date of October 2008 (**Reference 4**). Although the requirement for PFC has caused some concern within the power-adapter industry, little discussion has occurred about the need for PFC in the lighting industry, even for much lower power levels. In lighting, unlike power supplies, the industry leads the regulatory industry in energy-efficient adoption. EDN

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California Energy Commission
www.energy.ca.gov

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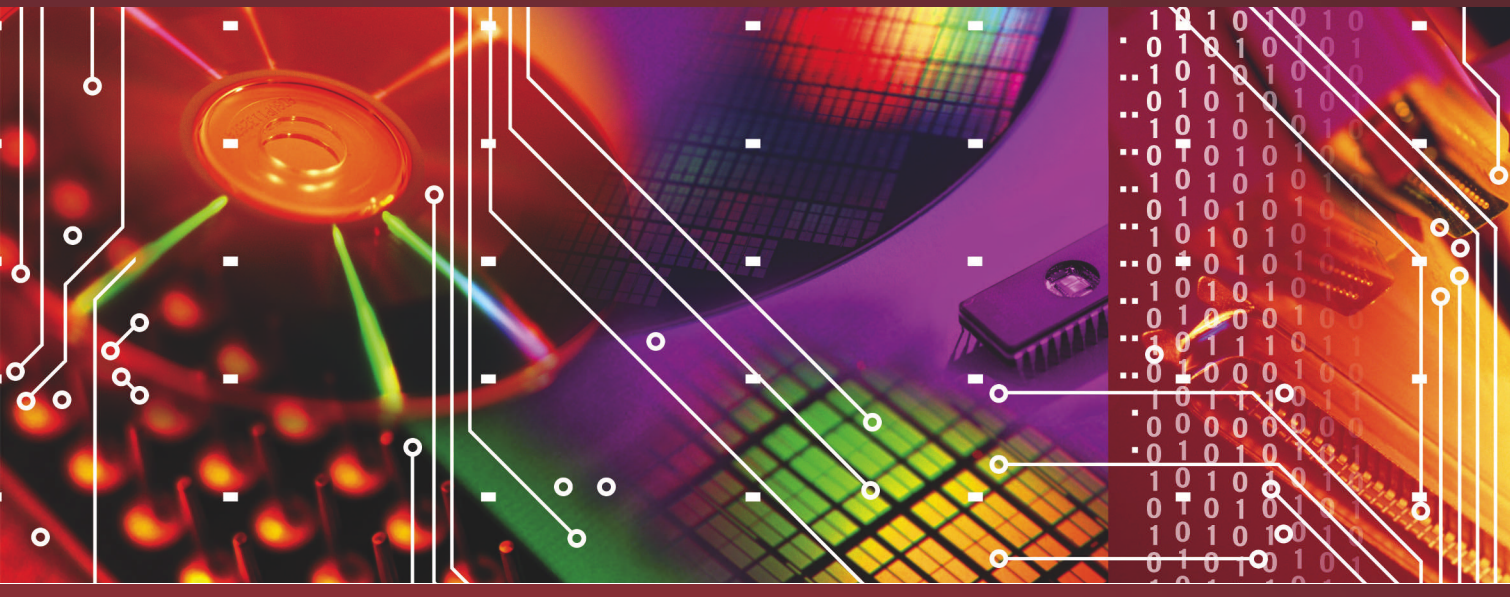

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# VMM application packages: the next level of productivity

A STANDARDIZED VERIFICATION METHODOLOGY INCREASES OUTPUT WITHOUT SACRIFICING DESIGN QUALITY.

The history of the EDA industry shows a clear, repetitive pattern. Designers develop new proprietary technologies, leveraging de facto and sanctioned industry standards; leading-edge users identify the most effective of these new technologies; and the industry turns the knowledge that users gain into the next set of de facto or sanctioned standards, allowing the creation of a set of newer technologies.

From the first netlist languages to Verilog to SystemVerilog, the functional verification of the digital-design segment of the EDA industry has seen—and continues to see—a rich sequence of ever-more-powerful standards. The methodology and associated support classes that the VMM (*Verification Methodology Manual*) for SystemVerilog describes were the next logical steps in this constant industrial evolution (**Reference 1**). Arising from proprietary methodologies that Synopsys (www.synopsys.com) and ARM (www.arm.com) developed, VMM has become a de facto standard for implementing constrained random-verification environments in SystemVerilog.

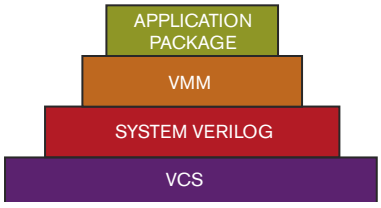


Figure 1 Just as VMM's (*Verification Methodology Manual*'s) creators built it on SystemVerilog, you can now build application packages on the infrastructure that the VMM provides.

A standard verification methodology enables the industry evolution to continue to the next level of productivity. Just as VMM's creators built it on SystemVerilog, you can now build application packages on the infrastructure that the VMM provides (**Figure 1**). User testbenches can then leverage the functions that those application packages provide, making them easier to implement correctly and increasing efficiency.

## IDENTIFYING APPLICATION PACKAGES

Designers build application packages, such as verification environments, on the generic VMM infrastructure. But unlike verification environments, which are specific to a design under verification, application packages are useful in implementing a variety of verification environments. Application packages must thus correspond to needs and requirements for verifying designs. Many years of verifying designs using the VMM and implementing VMM-compliant verification intellectual property—and many customers who do the same—helped Synopsys identify application packages that can boost the productivity of implementing VMM-based verification environments.

Almost all verification environments share some requirements. For some of these requirements, a simple extension of the VMM standard library is sufficient. For example, every verification environment must determine when it is proper to terminate a simulation. To that effect, VMM creators added a new utility class, vmm_consensus, to the VMM standard library. Some of these requirements require additional methodology statements, which new utility or base classes support. For example, the new VMM environment-composition package lets you reuse block-level environments in system-level environments. Another example is the RAL (register-abstraction-layer) package, which provides an object-oriented mechanism for accessing fields, registers, and memories regardless of their physical locations.

Verification environments share some requirements and use them to verify designs in application domains. An application domain with a large number of designs creates the opportunity for additional application packages. For example, a data-stream-scoreboarding package greatly facilitates the implementation of self-checking structures for networking and DSP applications. Another example is the memory-allocation-management package, which facilitates the allocation of memory buffers for configuring and verifying DMA and memory-controller applications.

## END OF TEST

The vmm_env::wait_for_end() method aims to let users implement how a verification environment detects the end of a test. Once the task completes, the user can cleanly shut down the verification environment, and a final accounting of all stimuli ensures that the environment has not accidentally lost any stimuli. You can detect the end of test by determining an absolute amount of elapsed time, counting a number of clock cycles, or observing a minimum number of transactions on an interface. These imperative end-of-test conditions are

easy to implement and suitable for directed test cases, but they are usually too simplistic for constrained random-verification environments.

When creating a constrainable random-verification environment, it is difficult to predict exactly how long various tests must run. Some trivial tests may need to run for only a few transactions. Corner-case tests may need to run for several thousand transactions. Furthermore, in a layered-verification environment, it is usually insufficient to count the number of occurrences of a significant event at a single location. For example, the number of packets you inject into the environment or the number of bus cycles you observe on an output interface will provide information about only the activity at that location. To safely end a test case in a layered-verification environment, it is usually necessary to wait for a combination of conditions: all of the generators generating the number of required transactions, all transactors sitting idle, no transactions remaining in transaction-level interfaces, or the scoreboard's observing enough activity, for example.

The VMM standard library provides a new utility class, vmm_consensus, to facilitate the identification of the test's end. As the name implies, this utility class implements a centralized decision-making mechanism that indicates when no participants object to the decision to end the test. This mechanism is perfectly scalable, allowing verification environments to grow—or for you to combine them—without affecting the complexity of the end-of-test decision. Yet, it transparently makes sure that the test ends as soon as but only when appropriate. For convenience, the vmm_env class now includes an instance of the vmm_consensus in the vmm_env::end_vote property.

The vmm_consensus utility class handles a variety of participants (**Figure 2**). Each participant can then object or consent to the final decision, independently of all other participants. The application can register channel instances as participants that implicitly consent when they are empty. It can register transactor instances as participants that implicitly consent while they are indicating the vmm_xactor::xactor_idle notification. The application can register on/off notifications as participants that implicitly consent while on or off. It can register other vmm_consensus instances as participants that implicitly consent when all of the other participants consent. You can also obtain generic participant interfaces for user-defined agreement or objection to the decision.

You need no longer implement a complex decision-making algorithm with multiple forked threads watching for different end-of-test conditions. Furthermore, because an object encapsulates the decision making, an environment can pass it to subenvironments, so the end-of-test decision process can scale as the complexity of the system-level-verification environment increases.

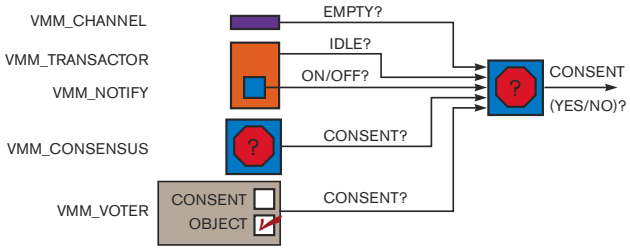


Figure 2 The vmm_consensus utility class handles a variety of participants.

Because the class is a generic decision-making utility, an environment can use different instances of the vmm_consensus to implement other decisions. For example, a transaction-level model could use the class to determine when all concurrent processing threads are done and thus can accept a new transaction for processing. A distributed simulation-sequencing mechanism could use it where various components indicate their objection or consent to proceeding further in the simulation.

## REGISTER-ABSTRACTION LAYER

Almost every design possesses registers accessible through a host processor. The first test cases written to verify almost every design are to determine that those registers operate as you would expect: that they reset to the appropriate value, that you can write writable bits, and that you cannot modify read-only bits. Unique to each design are the number of registers, the fields that compose them, whether you can write or read fields, and the physical protocol you use to write or read them.

When a design contains a few dozen registers, you can manually create—and, more important, maintain—the test cases and firmware-emulation routines. Using symbolic values for addresses and bit offsets can compensate for the maintenance effort. But when the number of registers is in the hundreds or thousands, creating and maintaining the register-correctness test cases and the firmware-emulation routines that the other functional tests use become overwhelming. The task gets even more daunting when it becomes necessary to migrate the block-level environment, firmware emulation, or tests to a system-level environment: The address of every register differs, and the physical interface you use to access the registers may no longer be available.

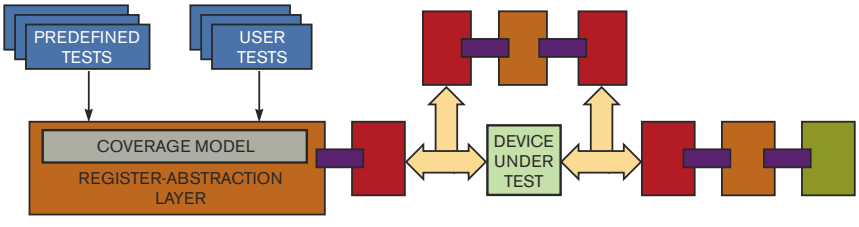


Figure 3 The register-abstraction layer isolates the upper layers of a verification environment and the test cases running on it from the implementation details of accessing the registers and memories in the design.

At this point, most verification teams determine that automatically generating some abstracted mecha-

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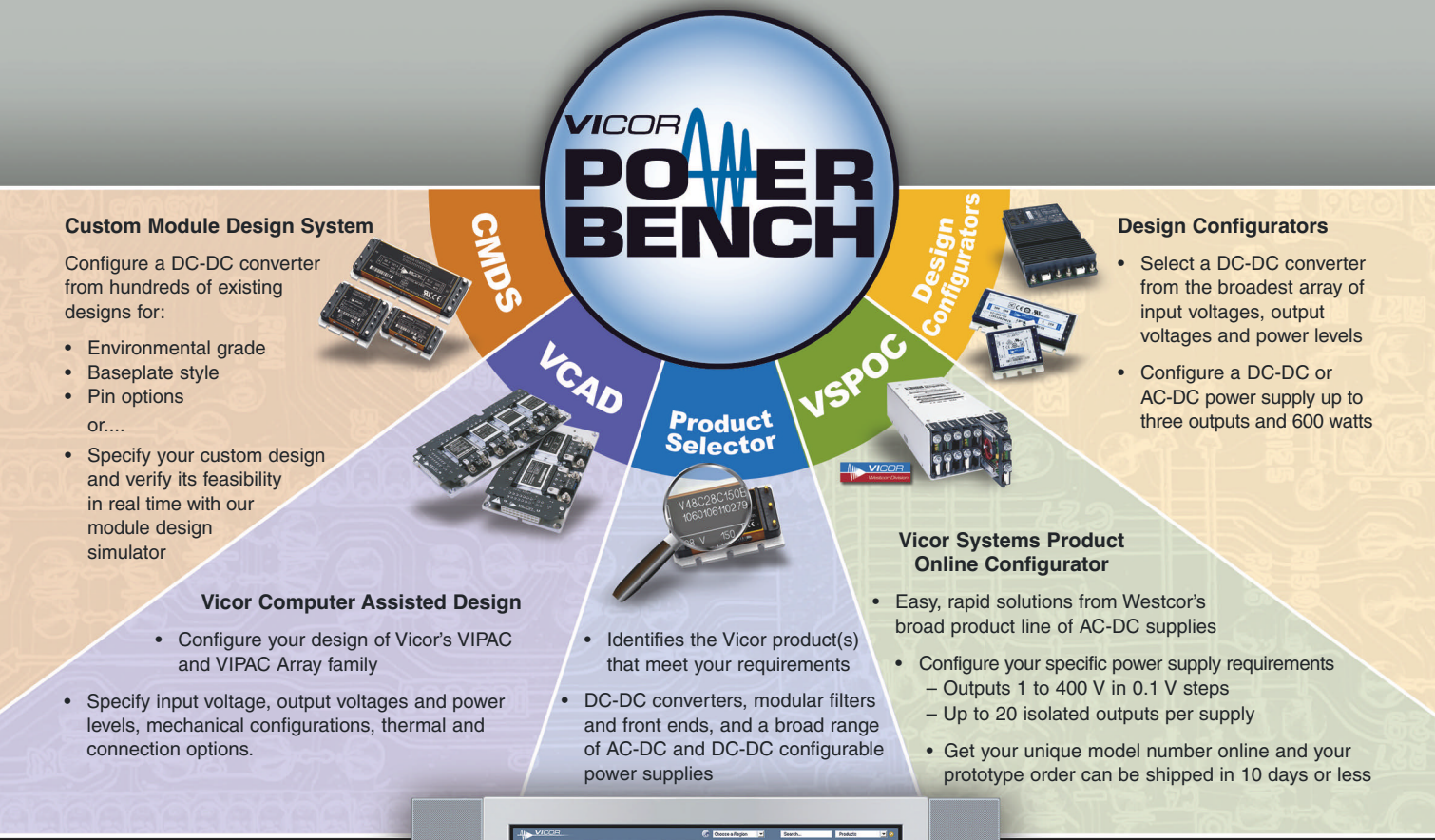


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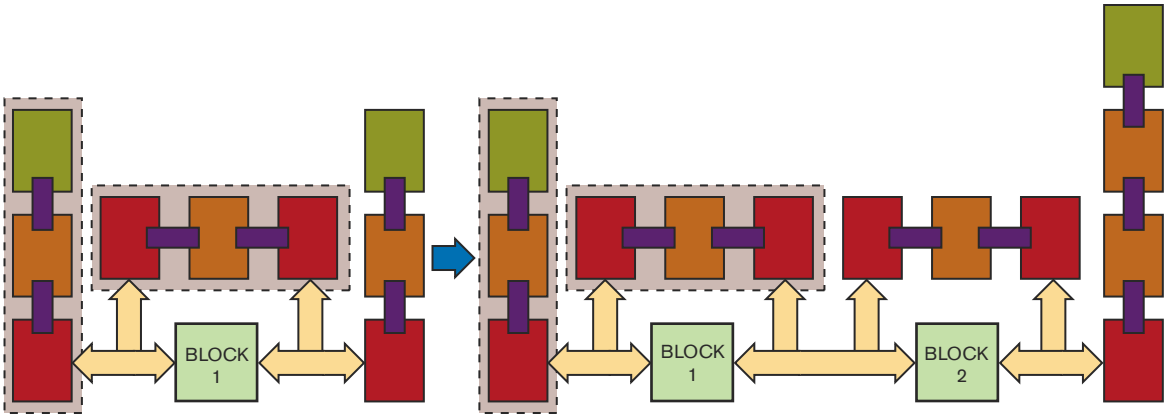


Figure 4 You can reuse entire networks of transactors from one environment to another.

nism for accessing and verifying the correct operation of the registers from a specification is more efficient than manually implementing and maintaining them. A generic register-access-abstraction mechanism, along with an automatic generation process from an executable specification of the registers in a design, dramatically reduces the threshold at which this automation becomes more productive.

The VMM RAL application package is a set of base classes, a code generator, and an executable-register-specification format that enables the automated generation of an object-oriented abstract register-access mechanism and predefined register-operational tests. The RAL isolates the upper layers of a verification environment and the test cases running on it from the implementation details of accessing the registers and memories in the design (**Figure 3**).

RAL simplifies not only the maintenance and verification of accessing registers and memories in the design, but also writing the code that needs to access them. Changes in physical interface, address, location, or bit offset of a field do not affect this simpler code, because the automatic generation of the design-specific RAL model based on any modification to the executable specification takes care of these nonfunctional implementation details.

The executable specification for the register that the RAL application package uses is congenial enough that you may use it as the primary register-specification vehicle and manually author and maintain it. However, you can just as easily generate it from register-specification documents, such as Excel spreadsheets or Word documents.

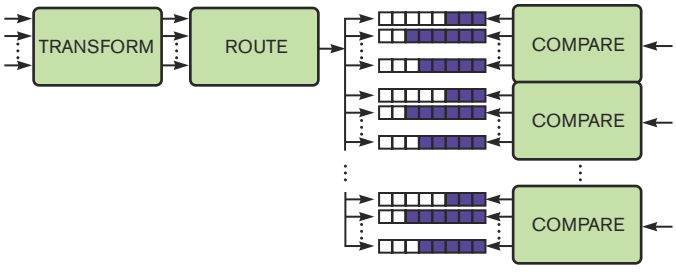


Figure 5 You can also use the VMM data scoreboard to verify multistream designs with user-defined data transformation and input-to-output stream routing.

## ENVIRONMENT COMPOSITION

The VMM defines the transactor as the unit of reusability, but more complex structures can be reusable. For example, a complete TCP/IP (Transmission Control Protocol/Internet Protocol) stack can be reusable, or the interface monitors and self-checking structure of an intellectual-property core can also be reusable. You can reuse entire networks of transactors from one environment to another (**Figure 4**).

Why not simply reuse entire environments? Why bother with subenvironments at all? Environments are specific to a design under verification. Unless a design is identical to the design you previously verified, the verification environment is not reusable. You must introduce configurability into the original environment to support its reusability in different contexts. For example, you would have to disable the entire stimulus stack on the SOC (system-on-chip)-bus side of an intellectual-property core to reuse the environment from the core level to the SOC level.

Rather than promote the creation of highly configurable verification environments, this application package takes a middle-of-the-road approach. Environments are design-specific and, thus, not reusable as is. However, you may make portions of those environments reusable and configurable. This ability simplifies the correct construction of both the reusable subenvironments and the environments that use them. But, should a complete environment be reusable, nothing prevents an author from encapsulating it as a reusable subenvironment.

Furthermore, subenvironments are not limited to encapsulating transactors, channels, and physical interfaces. They can also encapsulate smaller subenvironments that you combine to create a subsystem environment. You can then reuse these subenvironments in system-level environments.

Creating reusable subenvironments entails more than simply wrapping transactors, channels, and physical interfaces in yet another class. It must be possible to configure the DUT (device-under-test) functions associated with the reused subenvironment within the new context, without modifying the block-level configuration code. The VMM

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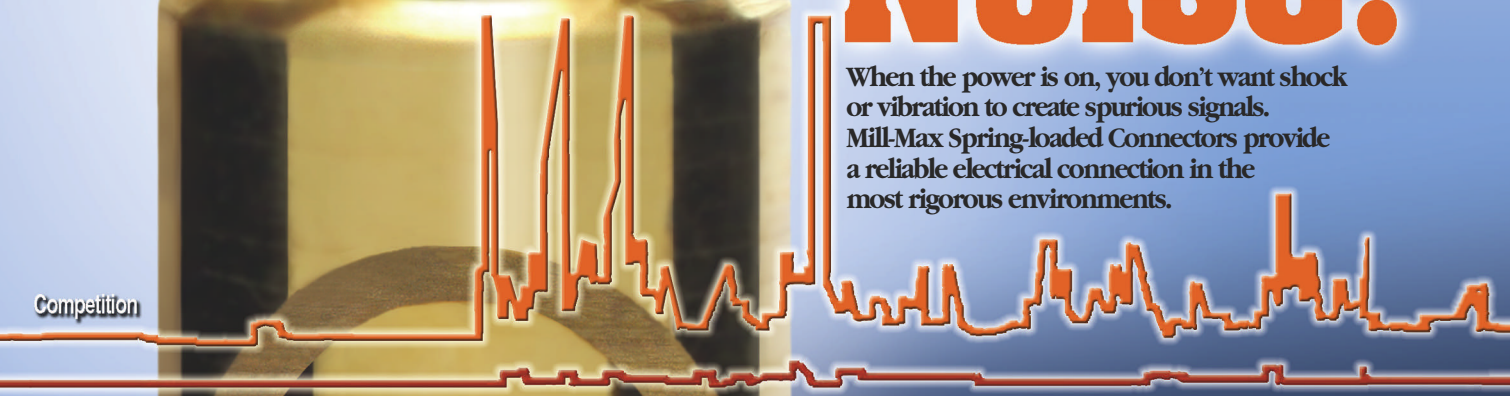


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RAL abstracts the configuration process in the subenvironment from the physical details of writing registers and memories. If the block-level functions require access to memory that the system may share at the system level, a memory-allocation manager must ensure that different blocks use different memory regions. Identifying the end-of-test condition must take into account the needs of the various subenvironments without requiring the author of the system-level environment to know the details of how a subenvironment determines it is time to end the simulation. The new vmm_consensus utility class allows the end-of-test condition to scale from block- to system-level environments.

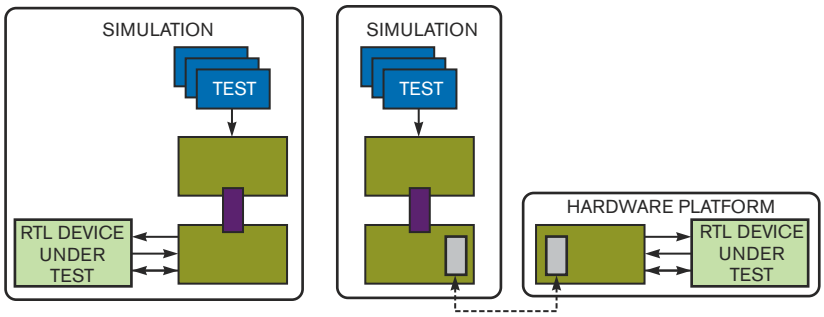
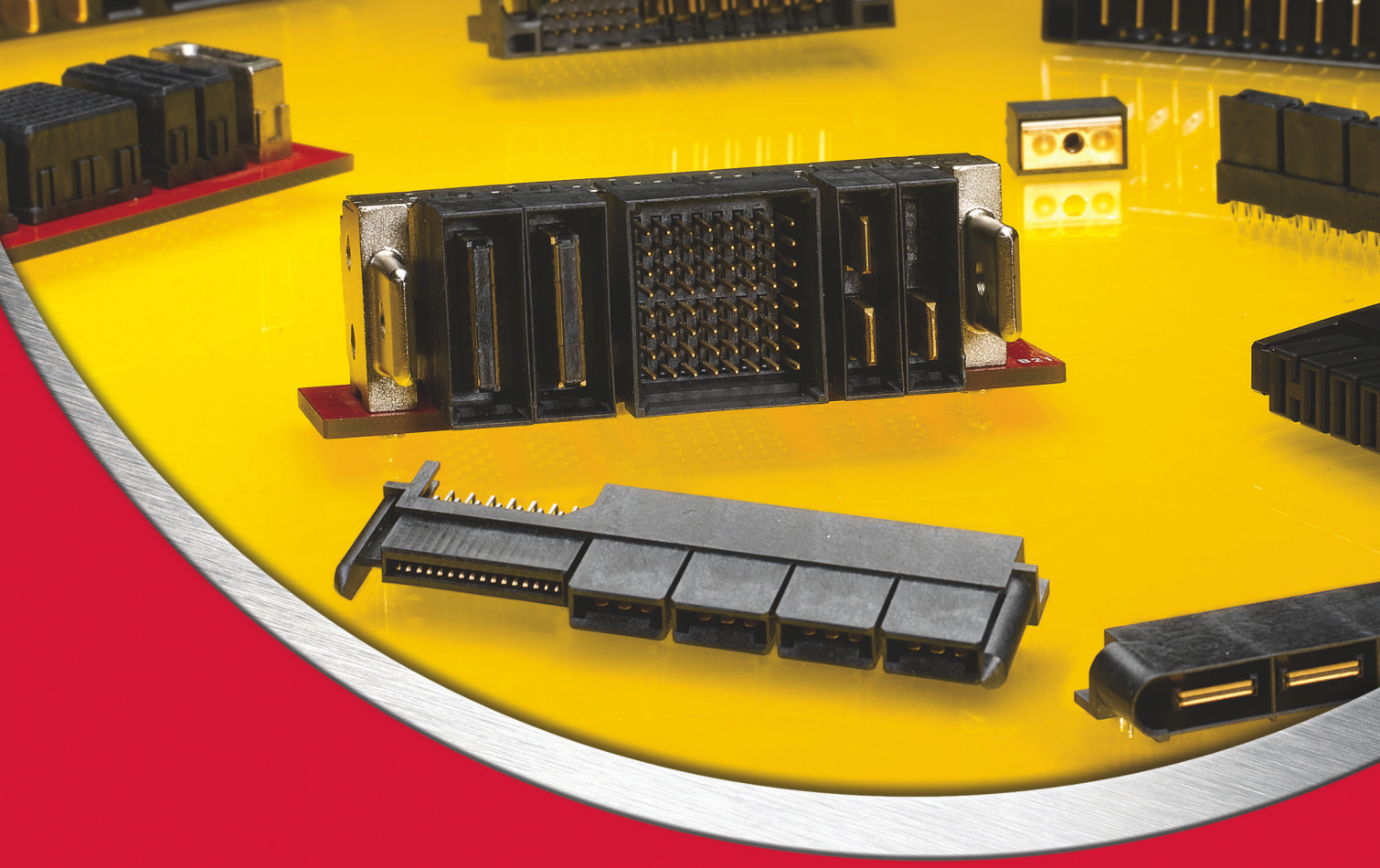



Figure 6 You can easily target a layered VMM-based verification environment from a pure software-simulation engine to a coemulation engine.

Reusing various structures from block- and system-level verification environments does not happen by accident. It is necessary to plan and build those block-level environments to create reusable structures. The VMM environment-composition package provides clear guidelines and support for implementing these reusable structures. Reusable subenvironments can greatly accelerate the creation and maintenance of higher level environments. With true reuse, you can even execute the development of block- and system-level environments in parallel, with the system-level environment automatically inheriting all updates and improvements you make to the portions of the block-level environments it reuses.

## DATA-STREAM SCOREBOARDING

Implementing the response-checking mechanism in a self-checking environment remains the most time-consuming task. The VMM data-stream-scoreboarding package facilitates the implementation of verifying the correct transformation, destination, and ordering of data streams. This package is intuitively applicable to packet-oriented design, such as modems, routers, and protocol interfaces. You can also use it to verify any design transforming and moving sequences of da-



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ta items, such as DSP datapaths and floating-point units.

You can use the VMM data-stream scoreboard out of the box to verify single-stream designs that do not modify the data flowing through them. For example, you can use it to verify FIFOs, MACs (media-access controllers), and bridges.

You can also use the VMM data scoreboard to verify multistream designs with user-defined data transformation and input-to-output stream routing (**Figure 5**). For example, it can verify an encryption engine as single stream or as a crypto transformation; as routers for multistream routing tables or with no transformation; and as data multiplexers with multiple input streams or encapsulation. The transformation from input data items into expected data items is not limited to one-to-one transformations. You can transform an input data item into multiple expected data items, such as segmenters, or no expected data items, such as reassemblers.

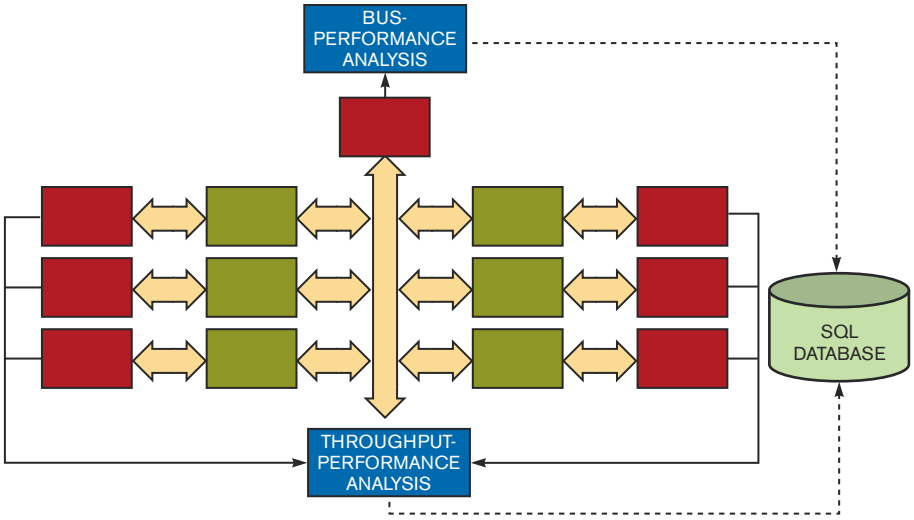


Figure 7 The VMM performance-analysis package can measure the performance of an SOC bus with multiple masters and multiple slaves or measure the overall throughput of a design.

The package provides three predefined "expect" functions: strictly in order, in order with losses, and out of order. But, should you require a different expect function, powerful iterator classes allow you to easily traverse the scoreboard-data structure without knowing the details of its implementation. You can also use these same powerful iterators to implement more complex prediction functions, such as reordering or multicasting.

Using the VMM data-stream scoreboard simplifies the creation of a self-checking structure by leveraging a proven and efficient set of data-structure and look-up functions. It also facilitates integrating the scoreboard with the rest of the verification environment. The VMM data-stream scoreboard is aware of the methodology for implementing the verification environment in which it will see use, and you can make VMM-compliant transactors aware of the scoreboard that will verify the response. The latest Synopsys version of the VMM library therefore includes predefined integration methods and macros to ease the task of getting the stimulus and observed response transactions to the scoreboard. Instead of manually extending, instantiating, and registering callback methods, VMM-compliant transactors now offer a predefined scoreboard-integration method. For example, you can now integrate the predefined VMM generators with a VMM data-stream-scoreboard instance using a single method call. Similarly, you can easily attach a VMM data-stream-scoreboard instance to the status information of a VMM notification.

## HARDWARE-ASSISTANCE LAYER

Simulations that require days of runtime can benefit from the performance of hardware-assisted verification. You map

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the design to a reconfigurable hardware platform, and the testbench remains on the simulator. The simulator and hardware platform then communicate to execute the simulation. The system realizes the greatest performance benefits when you also map a portion of the testbench to the hardware platform, alongside the design, and you minimize the frequency and amount of communication between the hardware platform and the simulator.

You can easily target a layered VMM-based verification environment from a pure software-simulation engine to a coemulation engine (**Figure 6**). The SCE-MI (Standard Coemulation Modeling Interface) industry standard offers a standard transaction-level communication mechanism between the simulated and the emulated layers of the testbench. However, the SCE-MI standard is currently only for C testbenches. The ability to reuse the SystemVerilog testbenches to verify the basic functions of the design and its components provides for greater productivity and shorter time to emulation.

The VMM hardware-abstraction-layer package provides a SCE-MI-like transaction-level interface mechanism between a simulated SystemVerilog testbench and emulated synthesizable bus-functional models, also written using SystemVerilog. The advantage of using a common language for both sides of the coemulation equation is that you can create a reference implementation that does not use a hardware platform. You can then use the reference implementation to develop the testbench and test cases as well as to reproduce failures that you observed on the emulator. This reference implementation, although significantly slower than a hardware platform, provides for a more flexible and integrated debugging capability, without tying up the hardware platform.

The VMM hardware-abstraction-layer package includes several guidelines for building coemulation testbenches and writing synthesizable command-layer transactors. It provides synthesizable message interfaces for synthesizable transactors and message-port classes to send messages to and receive messages from the emulated transactors. These interfaces and classes encapsulate the platform-specific message-passing mechanism, which can be SCE-MI, and render the verification environment portable to hardware-assistance platforms.

## PERFORMANCE ANALYZER

Functional coverage, which encompasses functional-coverage points in cover-group statements or coverage properties, measures the occurrence of simple singular events. When an event happens, the system records it. The simple fact that an event has occurred is enough to satisfy functional-coverage points.

But singular events are just one type of functional-coverage metric. The functional correctness of many designs requires the collection of statistical-coverage metrics, such as minimum, maximum, and average memory-request latencies or average and peak bus usage.

The VMM performance-analysis package enables the col-

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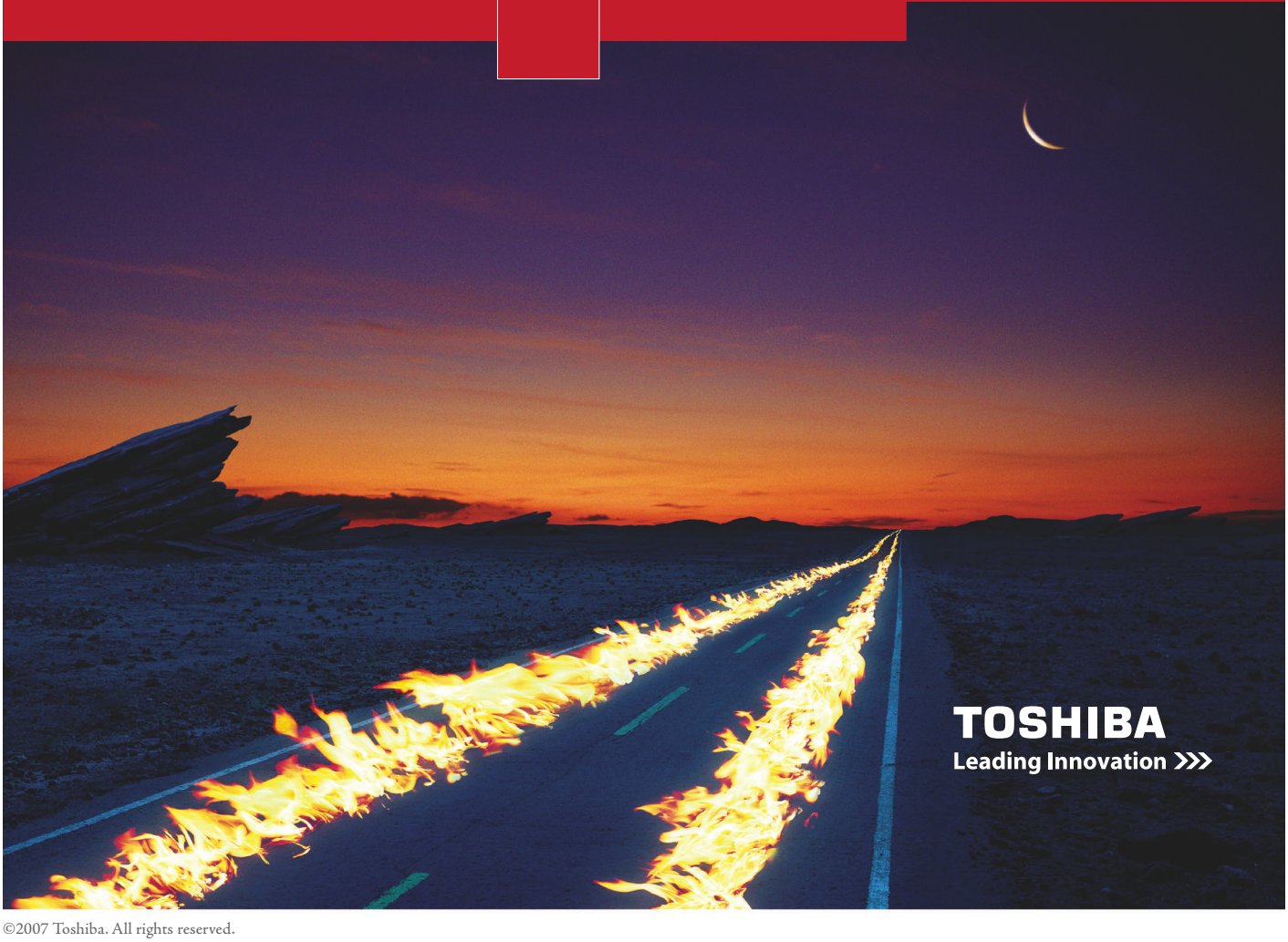


lection of statistical-coverage metrics. It can measure the performance of any resource that you use over time. Multiple initiators can use the resource, and multiple targets may provide the resource. For example, you could use it to measure the performance of an SOC bus with multiple masters and multiple slaves. You could also use it to measure the usage of a shared memory or an arbiter of the overall throughput of a design (**Figure 7**).

A simulation can contain several performance-analyzer instances, each measuring different performance aspects. You can merge the performance metrics you collect during concurrent simulation runs of a regression suite to obtain overall performance measurements across all of the simulations.

The definition of useful work and when that work starts, stops, resumes, and eventually completes are up to the user, as is the measure of usefulness of that work. Users can measure performance with respect to simulation time, number of clock cycles, or any other gauge of duration the user chooses. You can thus use the VMM performance-analysis package to measure any activity that occurs, such as bus usage, memory-subsystem response, or interrupt servicing, over time. The performance analyzer keeps track of the metrics—whatever they signify to the user—and allows the system to record, merge, and report them.

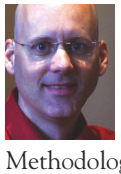
The system verifies the functional correctness of a design using scoreboarding techniques or reference models. When exploring the architecture of a design, functional correctness also includes meeting the performance requirements of the design. You can use the performance-analysis package to determine the performance correctness of a chosen architecture on a transaction-level or stochastic model of the design architecture or on an RTL (register-transfer-level) model.

Standardizing a common verification methodology offers the opportunity for developing functions at a higher level of abstraction. The VMM application package allows a verification team to increase its productivity without sacrificing the quality of the design under verification. EDN

## REFERENCE


1 Bergeron, Janick, Eduard Cerny, Alan Hunter, and Andy Nightingale, *Verification Methodology Manual for SystemVerilog*, Springer, 2005, ISBN 978-0-387-25538-5.


## AUTHOR'S BIOGRAPHY



*Janick Bergeron helps define the state of the art in functional-verification methodology and the tools that support it. He is the author of* Writing Testbenches Using SystemVerilog, *co-author of* Verification Methodology Manual for SystemVerilog, *and the moderator of the Verification Guild. Before joining Synopsys, Bergeron was chief technology officer of Qualis Inc and a member of the scientific staff at Nortel Networks. He holds a master's degree in business administration from the University of Oregon (Eugene, OR), a master's degree in electrical engineering from the University of Waterloo (Ontario, Canada), and a bachelor's degree in engineering from the Université du Québec à Chicoutimi (Quebec, Canada). He has been with Synopsys since 2003.*

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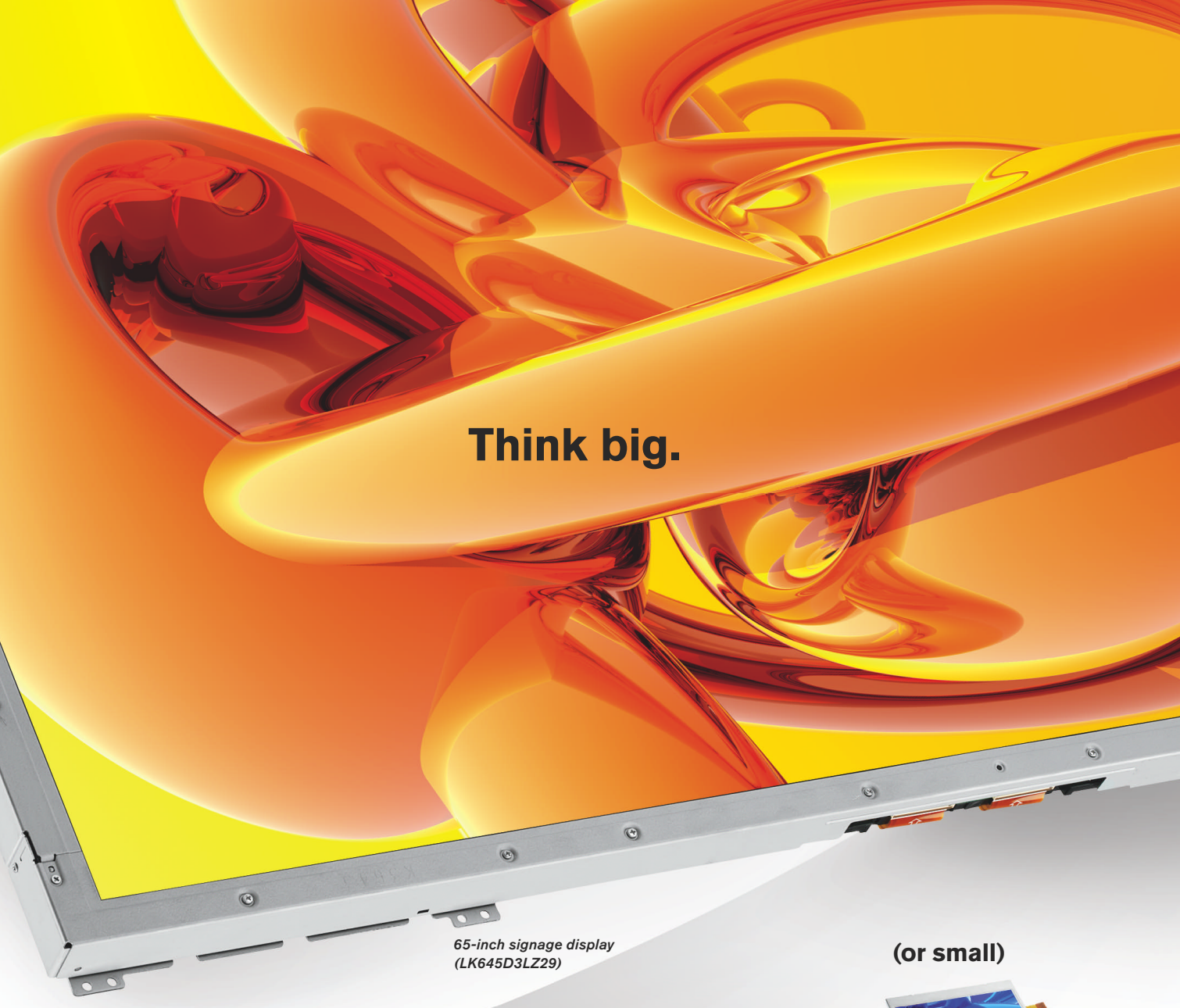

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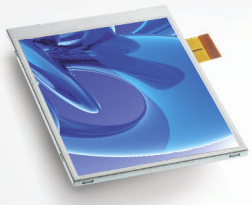

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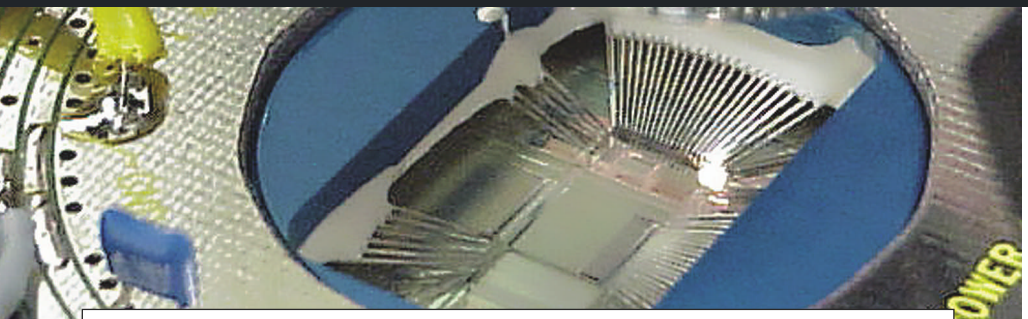
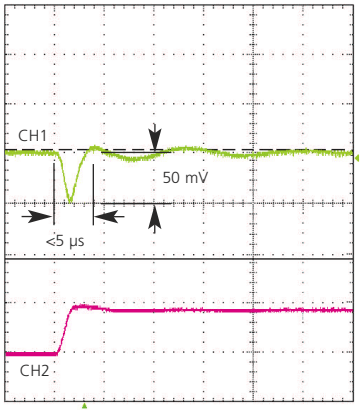


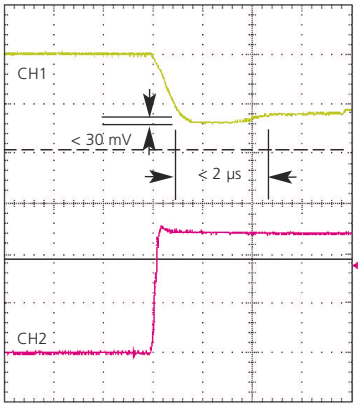
### Load Step Recovery




CH1: $V_{OUT}$ 50 mV/div
CH2: $I_{OUT}$ 50 A/div
Timebase: 5 µs

*48 $V_{IN}$, 1.2 $V_{OUT}$, 0-40 A at 10 A/µs*
*Less than 50 mV undershoot and recovery*
*in <5 µs using 330 µF ceramic $C_{OUT}$.*

### Load Line Recovery




CH1: $V_{OUT}$ 100 mV/div
CH2: $I_{OUT}$ 40 A/div
Timebase: 1 µs

*48 $V_{IN}$, 1.2 $V_{OUT}$, 0-100 A at 600 A/µs*
*Less than 30 mV undershoot and recovery*
*in <2 µs using 220 µF ceramic $C_{OUT}$.*

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| P048F048T24AL | 48 | 36 - 75 | 240 | 96.0 |
| P045F048T32AL | 48 | 38 - 55 | 320 | 97.0 |

| VTM Model No. | $V_{OUT}$ Nominal (V) | $V_{OUT}$ Range (V) | Output Current (A) | Efficiency @ 50% Load (%) |
|---|---|---|---|---|
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DESIGN BRIEF

# Simultaneous Power-Down Sequencing with Linear Regulators

By **Jeff Falin**
Senior Applications Engineer

## Introduction

In the past, ensuring successful power up for DSPs and FPGAs in electronic equipment was a challenge. The most recent DSPs and FPGAs have more relaxed requirements for core and I/O power up/down. However, a few still specify power-up ramp rates and recommend sequential sequencing for predictable and repeatable startup. Even fewer specify power-down requirements, including ramp rates and/or sequences. In most cases, the ultimate goal of these requirements is to ensure that the DSP and FPGA power rails do not have a larger differential voltage than that for which they were designed, even during the brief periods at power up/down. Otherwise, immediate or cumulative damage to internal circuits, which reduces long-term reliability, can occur. Therefore, the ideal method for DSP and FPGA power up/down is for all rails to rise and fall at the same time and rate.

Two or more power-rail ICs are said to have been simultaneously sequenced on power up when they track one another with the same rising dv/dt, and the lower rail stops at its regulated voltage while the upper rail continues to its higher regulated voltage. Various devices, including the TPS74301 linear regulator, have a tracking input to provide simultaneous power-up sequencing. Simultaneous sequencing on power up/down is implemented by replacing the converter's error-amplifier reference voltage with the tracking input signal while the signal is less than the reference voltage. However, for power-down sequencing to work, the converter must have circuitry to pull down the output under light load. Switching converters such as the TPS54x80 family can easily pull down the output by modulating the duty cycle. Most linear regulators do not have pull-down circuitry; so, even though the linear regulator tries to lower the output voltage, it must wait for the output capacitor to discharge through the load resistance. Figure 1 shows a block diagram of the TPS74301 configured to track the 3.3-V rail from a TPS54610. See Reference 1 for a complete schematic of TPS54xxx devices.

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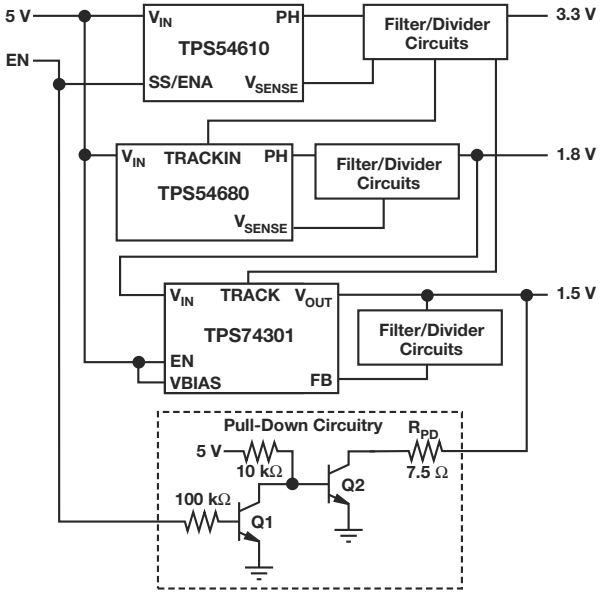


Figure 1. Block diagram of TPS74301 providing power-up/down sequencing

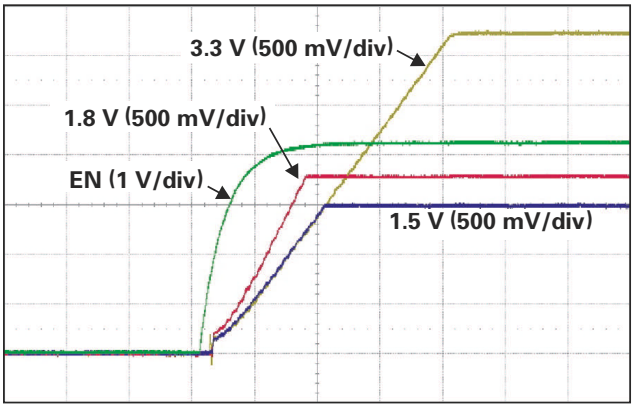


Figure 2. TPS74301 1.5-V output with power-up sequencing

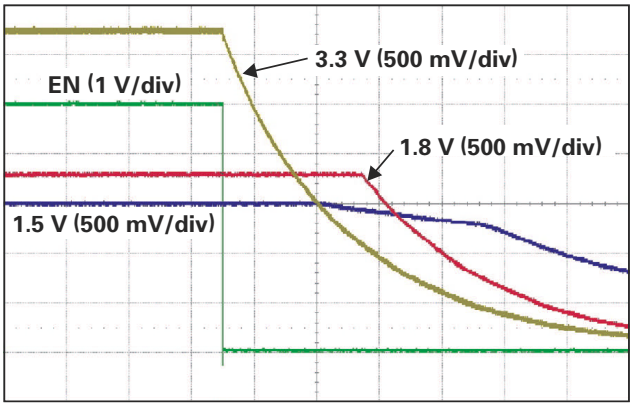


Figure 3. TPS74301 1.5-V output without power-down sequencing

Figure 2 shows simultaneous power up of the 3.3-V and 1.5-V rails. Figure 3 shows that, with the pull-down circuitry (low-cost, bipolar transistors Q1 and Q2 and their supporting components) removed, the TPS74301 output voltage does not track down because the power-down load resistance is too high. The pull-down circuitry shown in Figure 1 adds the pull-down resistor, $R_{PD}$, in parallel with $R_{L2}$, which lowers the regulator's load resistance and its RC time constant ($R_{L2} \times C_{O2}$) during power down. This means that the TPS74301 output will track down as shown in Figure 4, since the $R_{PD} \parallel (R_{L2} \times C_{O2})$ time constant is less than the $R_{L1} \times C_{O1}$ time constant.

The circuit in Figure 5 shows how to make all versions of the TPS74x01 family achieve "pseudo" simultaneous power-up/down sequencing by having $V_{OUT}$ follow $V_{IN}$. When $V_{IN}$ is less than the sum of the output voltage and the regulator's dropout voltage ($V_{DO}$) for a given output load, the regulator's pass element is operating in dropout. Therefore, if the load during power up/down is heavy enough, the regulator's output voltage could be below the voltage being tracked by $V_{DO(max)}$. Note that the soft-start capacitor, $C_{SS}$, must be set so that the TPS74x01 output ramps up faster than $V_{IN}$.

Please see Reference 2 for the complete version of this article, which shows waveform examples for two TPS74x01 devices with a 1-Ω load and one device with no load.

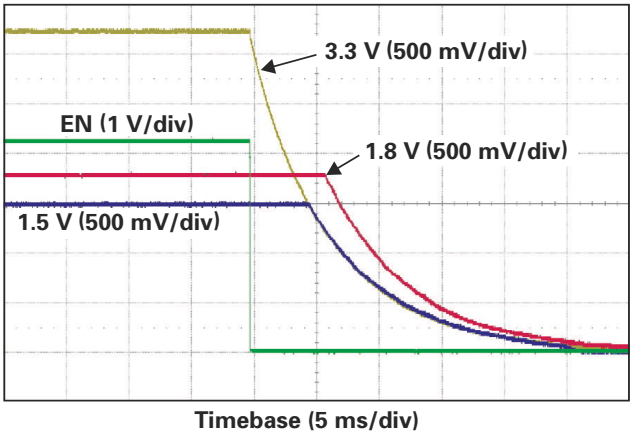


Figure 4. TPS74301 1.5-V output with power-down sequencing

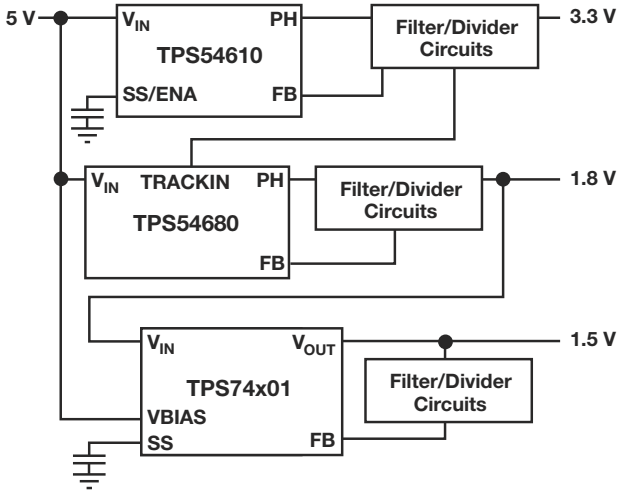


Figure 5. Block diagram of TPS74x01 providing pseudo power-up/down sequencing

## Conclusion

The TPS74x01 family of linear regulators easily provides simultaneous power-up sequencing and, with the assistance of simple pull-down circuitry and/or careful sizing of the load resistance at power down, provides two different methods for achieving simultaneous power-down sequencing.

## References

1. "TPS54680EVM-228 6-Amp, TPS54880EVM-228 8-Amp, SWIFT™ Regulator Evaluation Module," User's Guide, Literature number: slvu077
2. View the complete article at http://www-s.ti.com/sc/techlit/slyt281

BY TAKASHI KANAMORI AND GEORGE PAPARRIZOS • SUMMIT MICROELECTRONICS

# USB battery-charger designs meet new industry standards

USB IS NOT JUST FOR DATA TRANSFER ANY MORE; THERE ARE TOO MANY GOOD REASONS TO USE IT IN SUCH APPLICATIONS AS CHARGING HANDHELD-DEVICE BATTERIES. NEW STANDARDS ADDRESS SUCH USES, AND NEW CONNECTORS AND ICs CAN MAKE SHORT WORK OF YOUR DESIGNS.

The USB (Universal Serial Bus) has become the industry's most pervasive connectivity technology, especially in portable, consumer devices. The broad adoption of this standard has initiated several follow-up efforts that respond to handheld devices' continuing need to have USB perform more functions than just USB 2.0-compliant data transfer. The industry has seen a growing trend toward using USB's power capabilities to charge batteries. In addition, increasing numbers of applications now take advantage of the USB OTG (On-The-Go) supplement, which allows device-to-device connectivity without the need for a PC host. Moreover, the increasing dominance of industrial design in system design calls for space-saving, low-profile PCBs (printed-circuit boards) and components that require new, slimmer interconnection technologies. To provide industry-standard approaches to these challenges and maintain USB's high level of consumer satisfaction, the USB-IF (USB Implementers Forum) has developed several new specifications (**references 1** and **2**).

In addition to these specifications, other initiatives have found ways to address similar challenges. The most influential of these initiatives has been China's new Telecommunications Industry Standard for mobile-telecommunication-terminal equipment (**Reference 3**). This standard aims to reduce consumers' handset costs, to provide interoperability of ac/dc-charging adapters, and to protect the environment by minimizing electronic waste. Under the new standard, compliant wall-mounted chargers provide a USB connector to ensure universal charging with all mobile phones. The standard also specifies safety and performance requirements that chargers and phones must meet.

## BENEFITS OF USB CHARGING

Most of today's computers and peripherals, including flash cards, digital cameras, cellular phones, printers, mice, and keyboards, use a USB port for data transfer. The USB 2.0 specification has expanded market opportunities by enabling data transfer at rates as high as 480 Mbps and maintaining attractive plug-and-play characteristics (**Reference 4**). In addition, the USB port's power capabilities make it a useful power source for millions of consumers.

One of the most popular applications of the USB port's power capabilities is charging of single-cell lithium-ion- and lithium-polymer-battery packs. Many users spend hours each day in front of a PC and therefore have USB charging at their finger tips—a great convenience. According to the USB specifications, a USB port can deliver a theoretical maximum of 500 mA at 5V±10%. By taking full advantage of USB's power capabilities as well as the need for high-speed computer access, some applications have been able to eliminate the need for an ac adapter and its associated cost. A great example is the MP3 player: A typical user connects an MP3 player to a computer to create or update the device's music list, so a USB port and cable are already in use for data transfer. Using the same setup for battery charging is a logical next step. Digital still cameras, portable GPS (global-positioning-system) devices, and smartphones further exemplify applications that require PC access for data uploads, such as pictures and contacts, and thus can benefit significantly from USB charging.

## NEW USB-CHARGING STANDARDS

The new Chinese standard introduces a variety of electrical and mechanical requirements that ensure battery-charging intercompatibility and safety. The standard requires new wall chargers to provide a connector that complies with the USB Type A specification (**Figure 1**). This mechanical implementation allows connection of mobile phones to any dedicated wall charger or computing USB port for battery charging. The

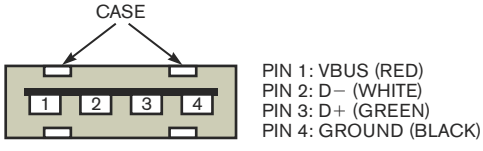


Figure 1 USB Type A connectors have four pins. The original function of pins 2 and 3 was data transmission. Newer standards also use these pins to enable communication between power controllers and power sources to establish such characteristics as maximum output current.

new wall chargers must be able to supply at least 300 mA but not more than 1.8A. This current range addresses both the low-cost and the high-performance product segments. The Chinese-government mandate also refers to a wall-charger-detection scheme, which requires detecting a short circuit between the D+ and D− terminals. Last, the new wall chargers' output voltage must be 5V±5%.

The new USB-IF battery-charging-specification revision 1.0, published in April 2007, introduces a provision that allows charging of a dead battery with 100 mA when the system is asleep until the system is awake, contrary to the original specification's 2.5-mA limitation. This higher current reduces wake-up time and eliminates the need for consumers to wait until the battery charges above the system-active level. This provision also introduces and defines three types of power sources for battery charging: a wall charger, a PC USB charger, and a host charger. These power sources look the same and have a USB mechanical connection. Therefore, the standard introduces a well-defined methodology for allowing the portable-device application to distinguish among them and take appropriate system actions.

In January 2007, the USB-IF also released the micro-USB specification for a next-generation USB connector (**Figure 2**). The development of this connector has enabled portable-system applications to further reduce space and profile without any performance or reliability compromises. Furthermore, the micro-USB-connector specification supports the current USB OTG supplement, which allows communication among portable devices without going through a host. Integrating OTG in new designs does, however, require use of the new connector, because micro-USB connectors don't support OTG. The first mobile phones with this new interconnect technology were announced in the second quarter of 2007, and industry leaders expect that, within a few years, the micro-USB technology will become the connectivity standard for portable devices.

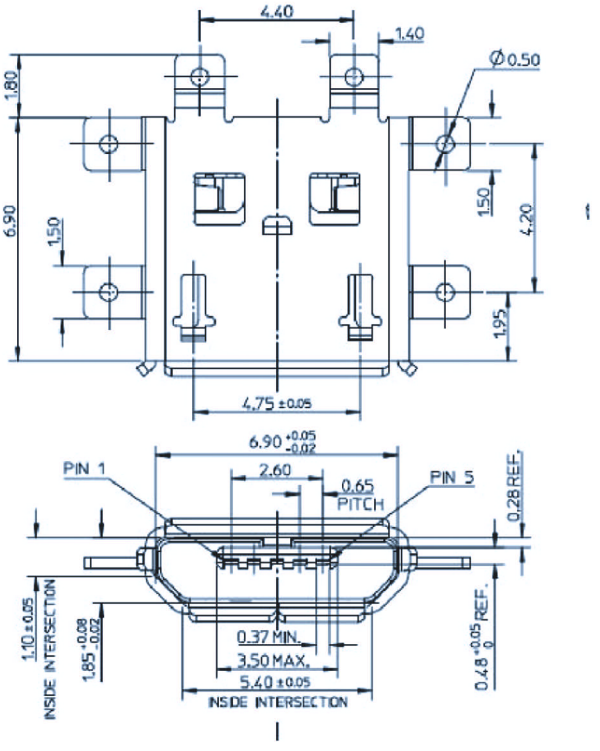


Figure 2 The new low-profile micro-USB connector allows cell phones to use computer-USB ports as well as dedicated chargers for both data interchange and battery charging (courtesy Molex Corp).

## POWER-SOURCE DETECTION

One of the most critical aspects of mobile-phone designs that must be compatible with the new standards is detection of the connected power source. Detection is critical because the new wall charger and USB ports will be mechanically identical to the older versions—that is, they both use USB Type A connectors—even though their power characteristics drastically differ. For example, when you connect a mobile handset to a USB port, the handset must fully comply with the USB 2.0 specification. In this case, the charger IC needs to initially limit the current to less than 100 mA and allow a 500-mA level only after completion of handshaking with the USB host or hub. On the other hand, when you connect a handset to a wall charger, charging can start immediately, and you should adjust the fast-charge current to a usually higher value that depends on the wall-charger rating.

Both the new Chinese and USB-IF standards provide guidelines for detecting the power-source type by reading the impedance between D+ and D−. More specifically, a compliant wall charger internally short-circuits D+ and D− and leaves the shorted node floating. Therefore, D+ and D− short together but do not connect to any part of the charger. The new Chinese standard doesn't specify short-circuit-detection mechanisms, whereas the USB-IF battery-charging specification 1.0 sets forth two alternative methods.

The USB protocol uses the D+ and D− signal lines to form


Figure 3 To control charging current, a new spec from the USB Implementers Forum calls for wall-mounted battery chargers to implement this design, which connects the USB connector's D+ and D− pins but does not otherwise connect them.

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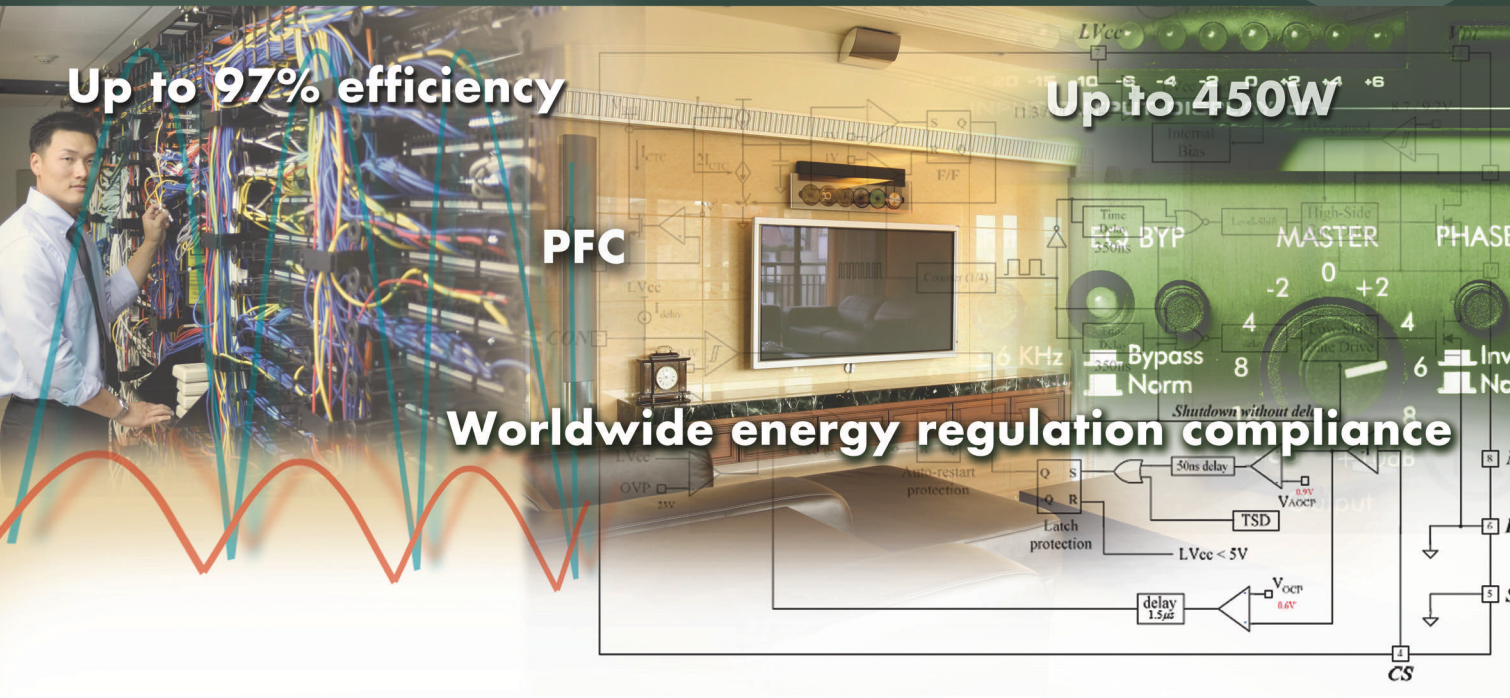


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Figure 4 If you use a PC's USB port for battery charging, the D+ and D− pins do not short together as they do in the wall-mounted charger. In addition, a 15-kΩ resistor connects each of the pins to ground.

a differential pair. D+ and D− carry binary data from an upstream port to downstream devices or from downstream devices to an upstream port. The USB 2.0 specification requires that 15-kΩ±5% resistors that connect to ground should terminate the D+ and D− lines at host or hub ports. A simple circuit detects whether the upstream port is a charger that the new standards specify (**Figure 3**). If the upstream port is a wall charger, D+ and D− should short together, and the shorted node should float.

When the upstream port is not a wall charger that one of the new standards specifies, D+ and D− do not short. Because the upstream-port connector is a USB-standard Type A device, the port is most likely a PC's USB port, which operates under a protocol that USB 2.0 specifies. Hence, D+ and D− require 15-kΩ±5% pulldown resistors at the upstream port (**Figure 4**).

## CURRENT LIMIT

Although the D+ and D− short-circuit-detection scheme can effectively identify a wall charger, the mobile device's charging-control circuit should determine the charger's current-carrying capability so that charging complies with safety standards. For instance, if the mobile's charging-control circuit tries to sink more current than the wall charger can furnish, an overcurrent condition results and activates overcurrent protection, which typically clamps the charger's output voltage, although some chargers may behave differently.

The Chinese standard specifies the maximum charger-output current as 300 to 1800 mA, whereas the new USB-IF battery-charging specification specifies a current range of 500 to 1800 mA. Therefore, the charger-current limit should lie between 300 or 500 mA and 1800 mA. To safely optimize charge current versus charge time, the charging-control circuit must identify the charger's current limit. Summit Microelectronics (www.summitmicro.com) has pending patent applications for making and applying this determination.

If you can't establish the optimum current, a safe design practice is to set the maximum-charge current to 300 mA, ensuring that the mobile phone operates safely with all compliant chargers whose current ratings lie between 300 and 1800 mA. A drawback is that such low charge currents yield long charging times, which negatively affect consumer perception. So, both standards require that wall chargers carry labels with relevant information, such as input and output current and voltage. It is therefore feasible to optimize the charge current for mobile-phone designs and to recommend the use of chargers with specific output-current ratings. For instance, setting the mobile device's sinking current at 800 mA for an 800-mAhr battery pack (1C rate) and recommending the use of chargers with no less than 800-mA output-current capability are effective ways to ensure sat-

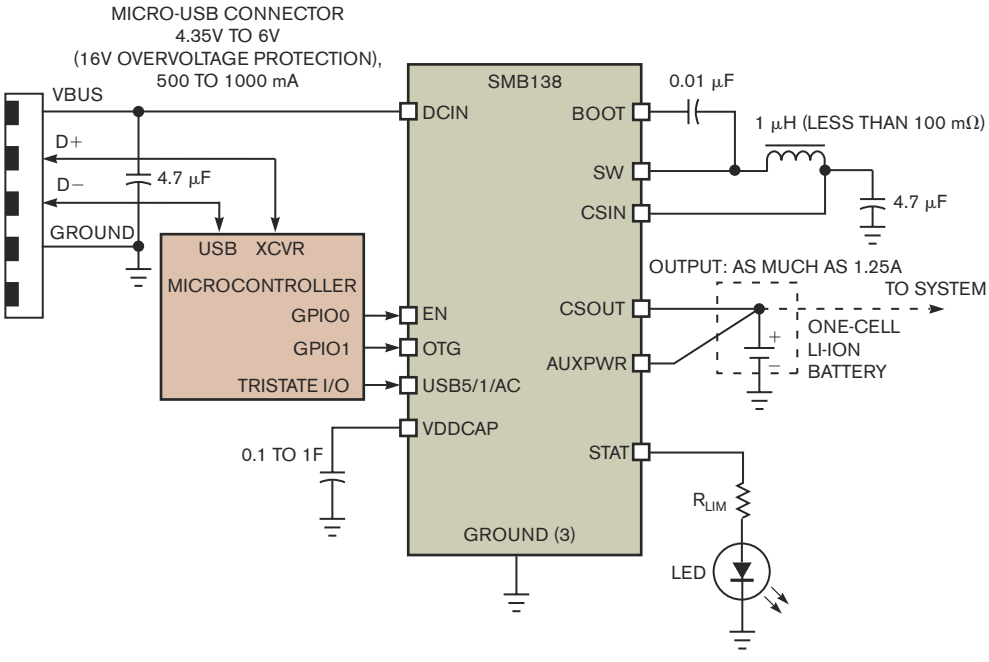


Figure 5 You need only one IC to meet the requirements of USB data transfer and charging control. This device also implements features that increase charging speed and ensure the application's safety.

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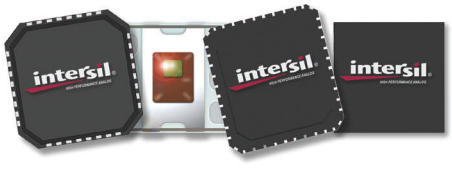


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isfactorily rapid charging. (The "1C rate" is the rate that will theoretically charge a battery to its capacity in one hour.)

## SAMPLE BATTERY-CHARGER IMPLEMENTATION

A typical charging approach is compatible with the several new standards (**Figure 5**). Summit Microelectronics' SMB138 switch-mode-battery-charger IC operates from 4.35 to 6V and is therefore compatible with the 5V±5% adapter-output voltage that the Chinese standard and the USB-power specifications specify (**Reference 5**). In addition, this charging IC incorporates input overvoltage protection that suspends operation when the charger voltage exceeds approximately 6.2V. Additional protection features, including battery-overvoltage and -overcurrent protection, meet the industry's strict secondary-safety requirements.

When the system detects a wall-charger connection with D+ and D− shorted, the system microcontroller or a discrete-switch implementation leaves the USB5/1/AC input floating, thereby allowing a programmable input current of 550 to 1250 mA. This operation allows for maximum-charge current and thereby minimum charging time in the fast-charge mode. If the system does not detect a short circuit between D+ and D−, it assumes that the mobile phone is connected to a desktop or notebook computer's USB port. To comply with USB 2.0, the microcontroller brings the USB5/1/AC input low, thereby limiting input current to less than 100 mA. Once the microcontroller has successfully performed the USB-enumeration procedure, the mobile phone, and therefore the charger IC, can draw as much as 500 mA from the USB port. To accomplish the current increase, the controller can bring the USB5/1/AC input pin high.

In addition to providing full compliance with the new standards, **Figure 5**'s implementation can provide additional value to the mobile-phone design. Unlike traditional linear-charging approaches, the basic operation of the SMB138's switch-mode architecture allows for an output charging current that can be significantly higher than the input current, resulting in shorter charging and a better consumer experience. This feature is beneficial when you use a USB port as a 500-mA-maximum power source. In addition, many of the new, compliant wall chargers are limited to current levels as low as 300 mA for reduced system cost and the lower cost associated with CCC (China Compulsory Certification). Such cost-reduction measures will be necessary to enable charger manufacturers to provide appropriately priced products for the broad consumer market.

When not in charging mode, the SMB138 can also provide the output voltage of 5V and current of more than 100 mA required for powering an OTG-compliant peripheral that connects to a mobile phone or digital camera. Integrating this capability eliminates the need for additional components, thereby reducing system cost and board space. Equipment designers can configure the SMB138 to operate in many modes and adapt it to many charging profiles. This versatility allows the use

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| CTLSH1-40M832D | 1.0 | 40 | Dual, Schottky | 3 x 2 x 0.9 | TLM832D |
| CTLSH2-40M832 | 2.0 | 40 | Single, Schottky | 3 x 2 x 0.9 | TLM832 |
| CTLSH3-30M833 | 3.0 | 30 | Single, Schottky | 3 x 3 x 0.9 | TLM833 |
| CTLSH5-40M833 | 5.0 | 40 | Single, Schottky | 3 x 3 x 0.9 | TLM833 |

**Transistors**

| Central Type No. | $I_C$ (A) | $V_{CBO}$ (V) | Description | TLM Size L x W x H (mm) | Package |
|---|---|---|---|---|---|
| *CTLT3410-M621 | 1.0 | 40 | Low $V_{CE(SAT)}$, NPN | 2 x 1 x 0.8 | TLM621 |
| *CTLT7410-M621 | 1.0 | 40 | Low $V_{CE(SAT)}$, PNP | 2 x 1 x 0.8 | TLM621 |
| CTLT853-M833 | 6.0 | 200 | High Current, NPN | 3 x 3 x 0.9 | TLM833 |
| CTLT953-M833 | 5.0 | 140 | High Current, PNP | 3 x 3 x 0.9 | TLM833 |

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| CTLM1034-M832D (NPN) | 1.0 | 40 | 1.0 | 40 | 3 x 2 x 0.8 | TLM832D |
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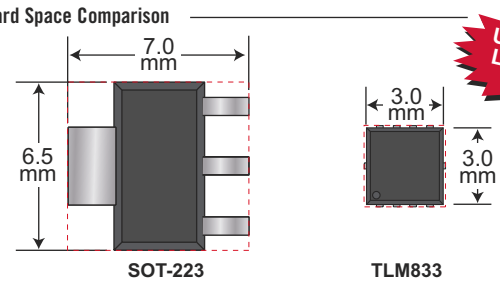


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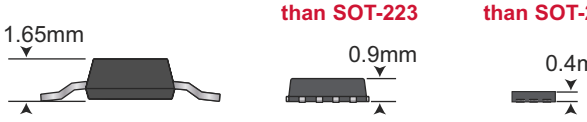


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of one type of IC in multiple products, even those with widely different system designs, battery types, and capacities. In addition, the advanced protection features provide primary and secondary protection and simplify compliance with strict safety standards, such as IEEE 1725.

USB's increasing popularity has resulted in several industry initiatives that respond to handheld devices' growing need for expanded USB capabilities. New battery-charging specifications introduce conditions and limits for allowing devices to draw current greater than what USB 2.0 specifies. The strengthening of supplemental specifications simplifies the use of USB without the need for a host. Requirements for slimmer industrial designs have resulted in the definition of new USB connectors that are poised to establish a new industry standard. All of these initiatives aim at maximizing consumer satisfaction by reducing cost, enhancing compatibility, and minimizing electronic waste. EDN



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LINEAR TECHNOLOGY

DESIGN NOTES

# Single Resistor Sets Positive or Negative Output for DC/DC Converter – Design Note 435

Jesus Rosales

## Introduction

Many electronic subsystems, such as VFD (vacuum fluorescent display), TFT-LCD, GPS or DSL applications, require more than just a simple step-down or step-up DC/DC converter. They may require inverting, noninverting converters or both. Designers usually resort to different regulator ICs to control various polarity outputs, thus increasing the inventory list. The LT®3580 solves this problem by controlling either positive or negative outputs using the same feedback configuration. It contains an integrated 2A, 42V switch and packs many popular features such as soft-start, adjustable frequency, synchronization and a wide input range into a small footprint. The LT3580 comes in an 8-pin 3mm × 3mm DFN or MSOP packages and can be used in multiple configurations such as boost, SEPIC, flyback and Cuk topologies.

## Sensing Output Voltage Has Never Been Easier

The LT3580 has a novel FB pin architecture that simplifies the design of inverting and noninverting topologies. Namely, there are two internal error amplifiers; one senses positive outputs and the other negative. Additionally, the LT3580 has integrated the ground side feedback resistor to minimize component count. To illustrate the benefits, notice how the schematics in Figures 1, 3 and 5 need only one feedback resistor.

A single sense resistor simply connects to the FB pin on one side and to the output on the other regardless of the output polarity, eliminating the confusion associated with positive or negative output sensing and simplifying the board layout. A user decides the output polarity he needs, the topology he wants to use and the LT3580 does the rest.

## Adjustable/Synchronizable Switching Frequency

It is often necessary to operate a converter at a particular frequency, especially if the converter is used in an RF communications product that is sensitive to spectral noise in certain frequency bands. Also, if the area available for a converter is limited, operating at higher frequencies allows the use of tiny component sizes, reducing the real estate required and the output ripple. If power loss is a concern, switching at a lower frequency reduces switching losses, improving efficiency. The switching frequency can be set from 200kHz to 2.5MHz via a single resistor from the RT pin to ground. The device can also be synchronized to an external clock via the SYNC pin.

## Soft-Start and Undervoltage Lockout

To alleviate high inrush current levels during start-up, the LT3580 includes a soft-start feature which controls the ramp rate of the switch current by the use of a capacitor from SS to ground.

The $\overline{SHDN}$ pin in the LT3580 serves two purposes. Tying it high or low turns the converter on or off. In situations where the input supply is current limited, has a high source impedance or ramps up/down slowly, the $\overline{SHDN}$ pin can be configured to provide undervoltage lockout through a simple resistor divider from $V_{IN}$ to ground.

## Boost Converters

A boost converter, shown in Figure 1, produces a positive output voltage always higher than its input. Figure 2 shows the efficiency graph for the boost converter in Figure 1 at a 4.2V input.



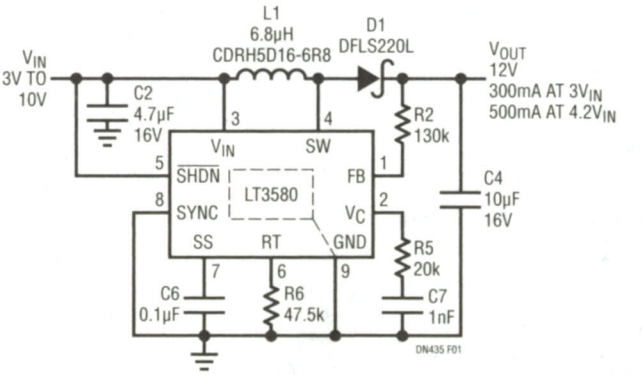


**Figure 1. 3V-10V to 12V, 300mA Boost Converter**

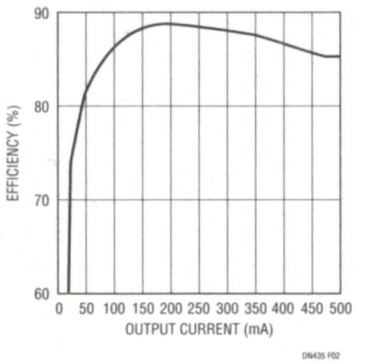


**Figure 2. Efficiency for the Figure 1 Converter at 4.2$V_{IN}$**

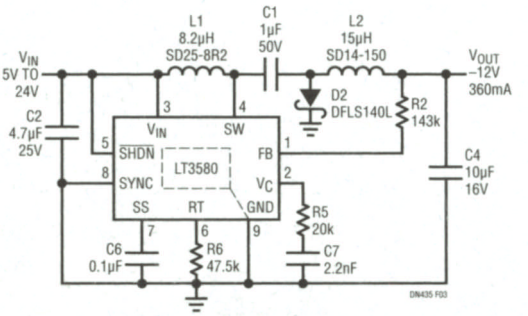


**Figure 3. 5V-24V to –12V, 350mA Cuk Converter**

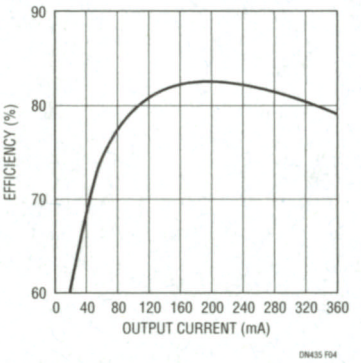


**Figure 4. Efficiency for the Figure 3 Converter at 5$V_{IN}$**

## Cuk Converter

Figure 3 shows a schematic for a Cuk converter, which produces a negative output with no DC path to the source. The output can be either higher or lower in amplitude than the input. The Cuk converter has output short-circuit protection, which is made more robust by the frequency foldback feature in the LT3580. Figure 4 shows the efficiency graph for the Cuk converter in Figure 3 at a 5V input.

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## SEPIC Converters

Figure 5 shows a SEPIC converter. A SEPIC converter is similar to the Cuk in that it can step up or step down the input; it offers output disconnect and short-circuit protection but produces a positive output. Figure 6 shows the switch waveform of the SEPIC converter during an output short-circuit event. Notice how the switching frequency folds back to one-fourth of the regular frequency as soon as the output voltage is shorted to ground. This feature enhances short-circuit performance for both Cuk and SEPIC converters.

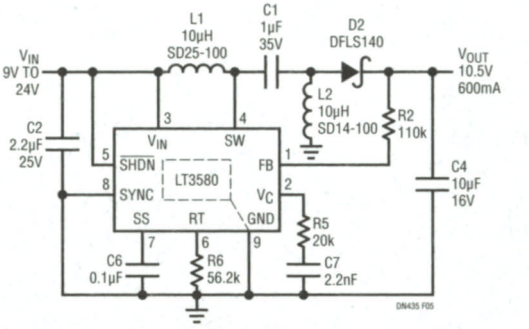


**Figure 5. 9V-24V to 10.5V, 600mA SEPIC Converter**

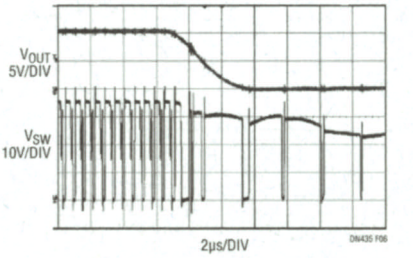


**Figure 6. Short-Circuit Event for the Figure 5 Converter at 24$V_{IN}$**

## Conclusion

The LT3580 features a unique feedback architecture that allows it to be configured as an inverting or noninverting converter. Now, the same device can be used to produce regulated voltages of either polarity, allowing for a reduction in inventory count. Its many additional features such as soft-start, adjustable switching frequency, shutdown, synchronizing capability, configurable undervoltage lockout, frequency foldback, external compensation and wide input range simplify the design of inverting and noninverting converters.

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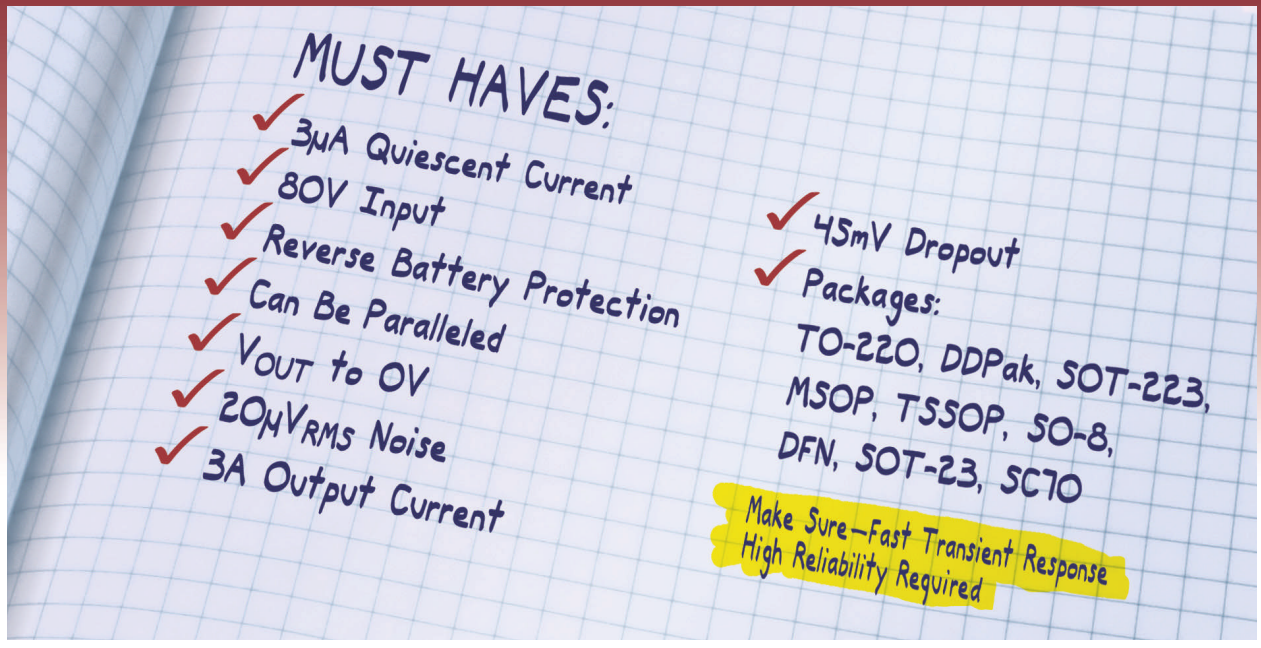
# High Performance LDOs




A new generation of high performance LDOs is now available from Linear. These LDOs are a generation beyond previous regulators in feature benefits and performance. These include ultralow quiescent currents to maximize battery life, low output noise to minimize potential interference, high input voltages for increased flexibility, protection features for rugged designs and an array of package options to facilitate both leaded and surface mount requirements.

## High Performance, Low-Noise LDOs

| Part No. | $I_{OUT}$ | Max. $V_{IN}$ (V) | Dropout Voltage (V) | Noise ($\mu V_{RMS}$) | $I_Q$ | Output Voltage (V) | Package (mm) |
|---|---|---|---|---|---|---|---|
| **LT®3009** | 20mA | 20 | 0.28 | 150 | 3µA | Adj. (0.6 to 19.5) | 2 x 2 DFN-6, SC70-8 |
| **LT3010/H*** | 50mA/50mA | 80 | 0.30 | 100 | 30µA | Adj. (1.275 to 60), 5 | ThinSOT™ |
| **LT1761** | 100mA | 20 | 0.30 | 20 | 20µA | Adj. (1.22 to 20), Fixed | ThinSOT |
| **LT1762** | 150mA | 6.5 | 0.30 | 20 | 25µA | Adj. (1.22 to 20), Fixed | MSOP-8 |
| **LT3012/H*** | 250mA/200mA | 80 | 0.40 | 100 | 40µA | Adj. (1.24 to 60) | 3 x 4 DFN-12, TSSOP-16E |
| **LT3013/H*** | 250mA/200mA | 80 | 0.40 | 100 | 65µA | Adj. (1.24 to 60) | 3 x 4 DFN-12, TSSOP-16E |
| **LT1962** | 300mA | 20 | 0.27 | 20 | 30µA | Adj. (1.22 to 20), Fixed | MSOP-8 |
| **LTC®3025** | 300mA | 5.5 | 0.05 | 80 | 54µA | Adj. (0.4 to 3.6) | 2 x 2 DFN-6 |
| **LTC3035** | 300mA | 5.5 | 0.045 | 150 | 100µA | Adj. (0.4 to 3.6), Fixed | 2 x 2 DFN-6 |
| **LT1763** | 500mA | 20 | 0.30 | 20 | 30µA | Adj. (1.22 to 20), Fixed | SOIC-8 |
| **LTC3025-1/-2** | 500mA | 5.5 | 0.075 | 80 | 54µA | Adj. (0.4 to 3.6)/1.2 | 2 x 2 DFN-6 |
| **LT3080**** | 1.1A*** | 36 (40 Abs Max) | 0.3+ | 40 | 1mA | Adj. (0 to 36)++ | 3 x 3 DFN-8, MSOP-8E, TO-220, SOT-223 |
| **LT1965** | 1.1A | 20 | 0.29 | 40 | 500µA | Adj. (1.20 to 19.5) | 3 x 3 DFN-8, MSOP-8E, TO-220, DDPak |
| **LT1963/A** | 1.5A | 20 | 0.34 | 40 | 1mA | Adj. (1.21 to 20), Fixed | DDPak, TO-220, SOT-223, SO-8 |
| **LT1764/A** | 3A | 20 | 0.34 | 40 | 1mA | Adj. (1.21 to 20), Fixed | DDPak, TO-220 |

*Tj = 140°C Operation (H-grade)
**Current-based Reference
***Can Be Paralleled
+Two-supply Operation
++Single-resistor $V_{OUT}$ Set

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# designideas

READERS SOLVE DESIGN PROBLEMS

## NE555 timer sparks low-cost voltage-to-frequency converter

Gyula Diószegi and János Nagy, Divelex Ltd, Budapest, Hungary

In 1971, Signetics—later Philips (www.philips.com)—introduced the NE555 timer, and manufacturers are still producing more than 1 billion of them a year. By adding a few components to the NE555, you can build a simple voltage-to-frequency converter for less than 50 cents. The circuit contains a Miller integrator based on a TL071 along with an NE555 timer (**Figure 1**). The input voltage in this application ranges from 0 to −10V, yielding an output-frequency range of 0 to 1000 Hz. The current of $C_1$ is the function of input voltage: $I_C=-V_{IN}/(P_1+R_1)$.

As the voltage on $C_1$ reaches two-thirds of $V_{CC}$, the 555's internal discharge transistor opens, and the voltage on $C_1$ returns to one-third the voltage of $V_{CC}$, the lower comparator threshold. At one-third this voltage, the discharge transistor switches off, and $C_1$ again starts charging. The NE555's output is high while $C_1$ is charging and low while $C_1$ is discharging. The product of the input voltage and the charging time of $C_1$ is constant. Because the discharge time is shorter than the charging time, the following **equation** results for the output frequency: $f_{OUT}\sim V_{IN}/(P_1+R_1)\times C_1\times 1/3V_{CC}$.

$P_1$ calibrates the relationship between the output frequency and the input voltage. Because the discharge interval is approximately 30 µsec, the accuracy of the voltage-to-frequency conversion decreases as the frequency increases. If you assign 100 Hz to −1V and 1000 Hz to −10V, the error of conversion ranges from 0.3 to 3%. If you use $P_1$ to calibrate the output frequency in the middle of the input-voltage range at −5V, then the conversion error will be less than 1.3% over the entire range. To improve performance, $C_1$ should have a low dissipation factor. You can diminish temperature dependence if $R_1$ has a low temperature coefficient and $P_1$ is a multiturn, ceramic-metal potentiometer. EDN

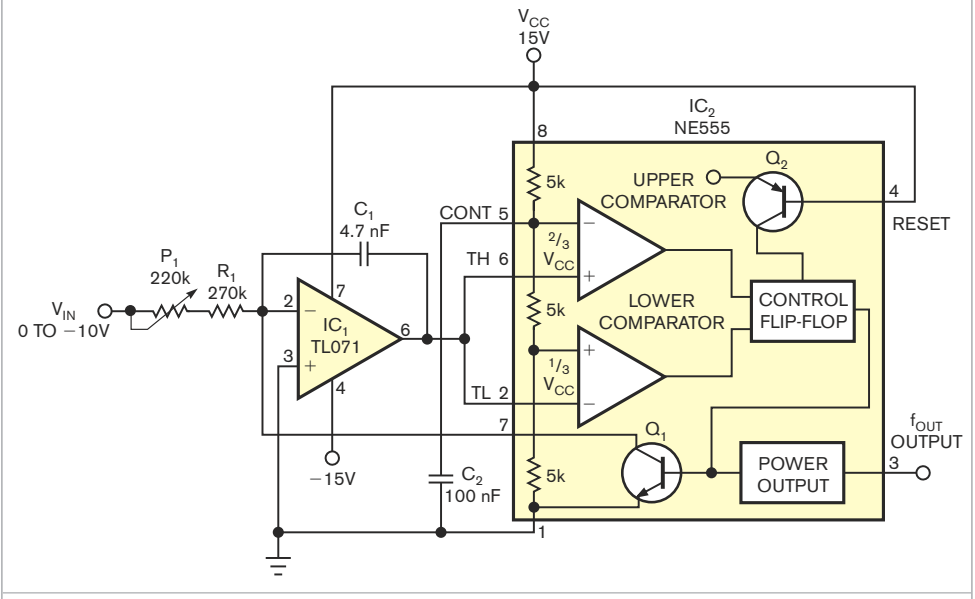


Figure 1 Preceding an NE555 timer with a Miller integrator yields a voltage-to-frequency converter that costs less than 50 cents.

### DIs Inside



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# Optoisolators compute watts and volt-amperes

W Stephen Woodward, Chapel Hill, NC

A decade or so ago, I designed a simple circuit that included a quad optoisolator arranged in a full-wave analog-multiplier bridge (**Figure 1**). It sensed and calculated watts of ac-power consumption and ignored any reactive component in the load. The circuit's principle of operation relies on the fact that the LEDs of the bridge, like any other device with a semiconductor junction, have a dynamic conductance that's directly proportional to current: approximately 19 mS (millisiemens)/A at 25°C. Both the line voltage and load-current-proportional sense voltage, which the 0.001Ω copper shunt develops, modulate this current. The approximately 0.4%/°C temperature coefficient of the copper compensates most of the temperature dependence of the LEDs' conductances.

The circuit in this Design Idea is an elaboration on that older circuit. It acquires not only watts, but also volt-amperes and so makes possible an estimation of power factor—watts divided by volt-amperes. The right-hand side of the circuit in **Figure 2** is simply a half-wave version of the older circuit. The left-hand side is similar but substitutes rectified-dc excitation of its half-wave bridge for the ac excitation of the left-hand side. The analog product of instantaneous load current times the average voltage optically couples to phototransistor $Q_4/D_4$, which $A_2$ amplifies and the $Q_5$ through $Q_8$ transistor array rectifies to provide an analog voltage proportional to load volt-amperes. EDN

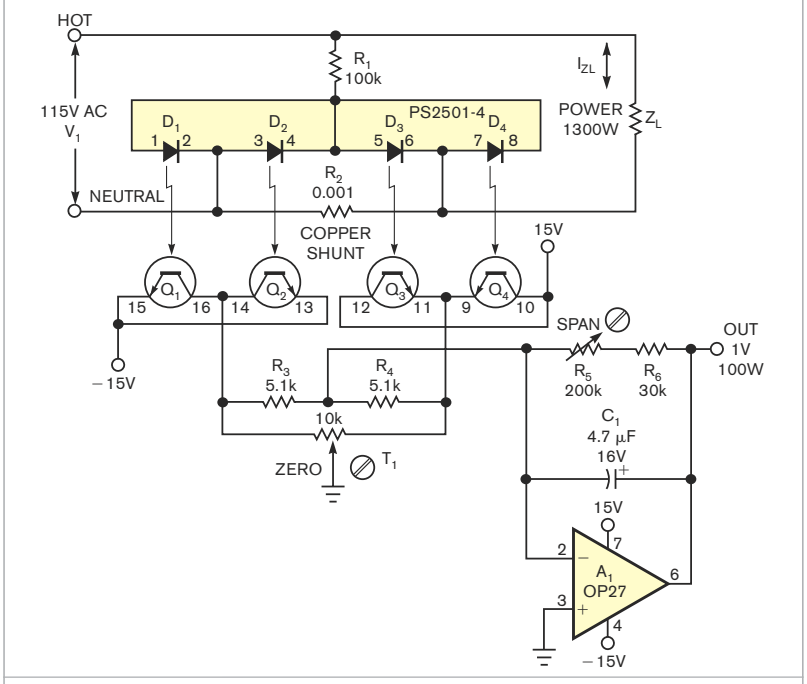



Figure 1 A quad optoisolator arranged in a full-wave analog-multiplier bridge senses and calculates watts of ac-power consumption and ignores any reactive component in the load.

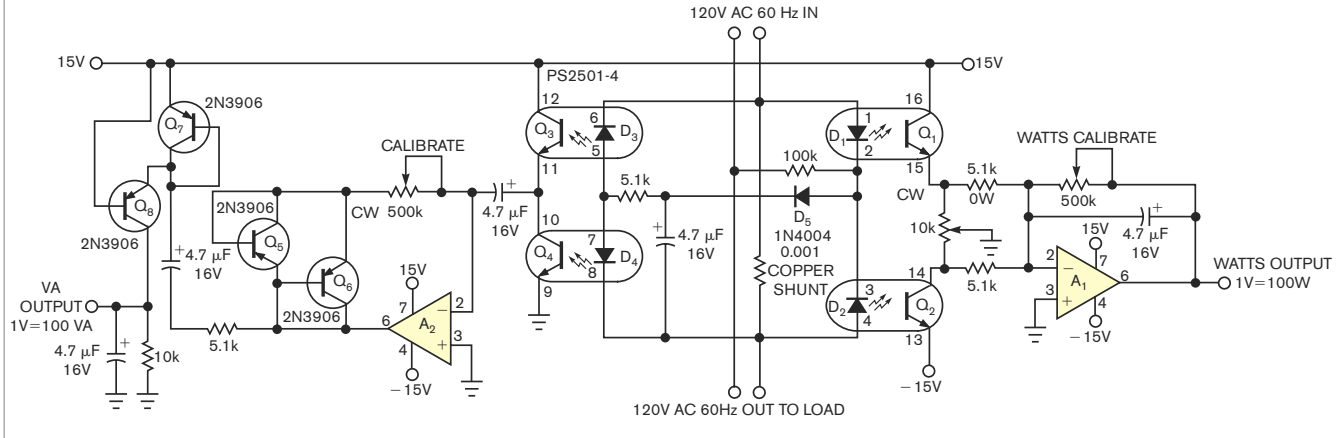
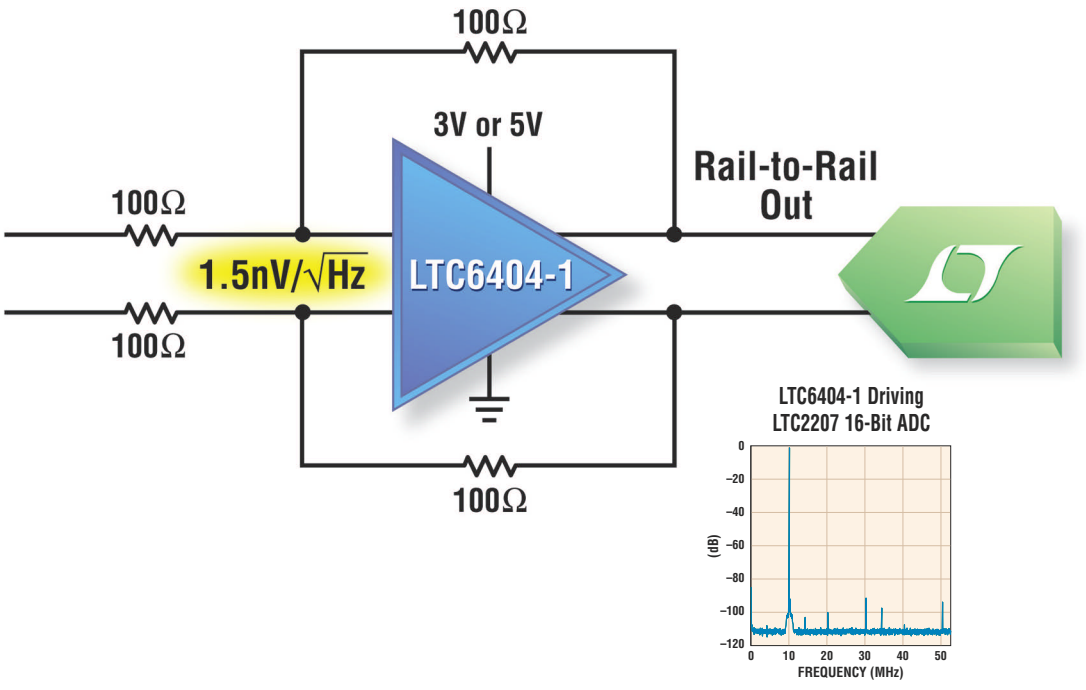



Figure 2 The right-hand side of this circuit is simply a half-wave version of the circuit in Figure 1. The left-hand side is similar but substitutes rectified-dc excitation of its half-wave bridge for the ac excitation of the right-hand circuit.

# Ultralow Noise ADC Driver

## 16-bits @ 10MHz

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| | LTC6403 | LTC6404 | LTC6406 | LTC6401 | LTC6400 |
|---|---|---|---|---|---|
| **Input Frequency Range** | DC-15MHz | DC-30MHz | DC-60MHz | DC-140MHz | DC-300MHz |
| **Gain** | R-set | R-set | R-set | 8, 14, 20, 26dB | 8, 14, 20, 26dB |
| **Distortion** | -95dBc @ 3MHz | -92dBc @ 10MHz | -72dBc @ 50MHz | -88dBc @ 70MHz | -81dBc @ 140MHz |
| **Noise** | 2.8nV/√Hz | 1.5nV/√Hz | 1.6nV/√Hz | 2.1nV/√Hz | 2.1nV/√Hz |
| **Supply Voltage** | 2.7V to 5.25V | 2.7V to 5.25V | 2.7V to 3.5V | 2.85V to 3.5V | 2.85V to 5.25V |
| **Supply** | 11mA | 27mA | 18mA | 45mA | 85mA |

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# Single-supply circuit measures −48V high-side current

Wenshuai Liao, Analog Devices, Beijing, China;
Stephen Lee, Analog Devices, Wilmington, MA; and
Yanhui Zhao, Beihang University, Beijing, China

The nominal −48V rail, which finds wide use in wireless base stations and other telecommunications equipment in network central offices, can vary from −48 to −60V. Measuring its current draw typically requires components that operate on ±15V dual supplies. Eliminating the negative supply would reduce system complexity and cost. This Design Idea uses an AD629 difference amplifier and an AD8603 operational amplifier, both from Analog Devices (www.analog.com), to measure current at −48 to −60V and operates from a single positive-power supply (**references 1** and **2**).

**Figure 1** shows how the AD629 and AD8603 measure current in the presence of a −48V common-mode voltage. The following **equations** demonstrate how the AD629 difference amplifier can condition voltages beyond its supply ranges: $V_{COM\_MAX}=20\times(V_S-1.2)-19\times V_{REF}$, and $V_{COM\_MIN}=20\times(-V_S+1.2)-19\times V_{REF}$. With a 5V reference, the common-mode input range is −71 to +121V. The current, I, flows through the shunt resistor, $R_S$, causing a differential voltage, which the difference amplifier senses. The AD629 has a fixed gain of one, so the output voltage is $I\times R_S+V_{REF}$. The AD8603 functions as a subtractor so that it can reject the common-mode voltage, $V_{REF}$, and apply gain to the signal of interest, $I\times R_S$. A factor of 20 amplifies the signal to span the 2.5V full-scale range of the ADC.

This Design Idea uses the AD8603 because it has low input-bias current and low offset drift. In addition, the rail-to-rail output allows it to share the same supply as the ADC. In this stage, the subtractor rejects the 5V common-mode signal from the voltage reference. The four resistors that form the subtractor must have matched ratios to obtain maximum common-mode rejection. If you cannot obtain tightly matched resistors, you can use an AD623 single-supply instrumentation amplifier in place of the AD8603, ensuring high common-mode rejection.

Offset, input-bias-current, and common-mode-rejection errors from both amplifiers result in a 163-mV maximum error at the output of the AD8603. This calculation assumes resistors with a 0.01% ratio match. The circuit was verified on the bench using 50-, 100-, and 200-mΩ shunts for $R_S$. EDN

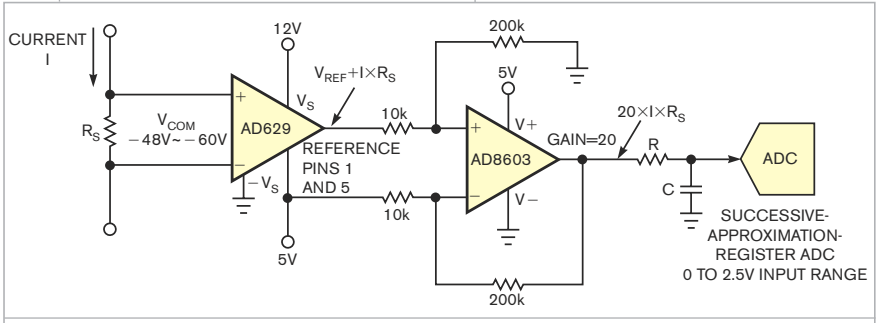



Figure 1 The AD629 and AD8603 measure current in the presence of −48V common-mode voltages.

## REFERENCES

1 "High Common-Mode Voltage, Difference Amplifier AD629," Analog Devices, 1999 to 2007, www.analog.com/UploadedFiles/Data_Sheets/AD629.pdf.
2 "Precision Micropower, Low Noise CMOS Rail-to-Rail Input/Output Operational Amplifiers AD8603/AD8607/AD8609," Analog Devices, 2005, www.analog.com/UploadedFiles/Data_Sheets/AD8603_8607_8609.pdf.

# Three-state switch interface uses one microcontroller pin

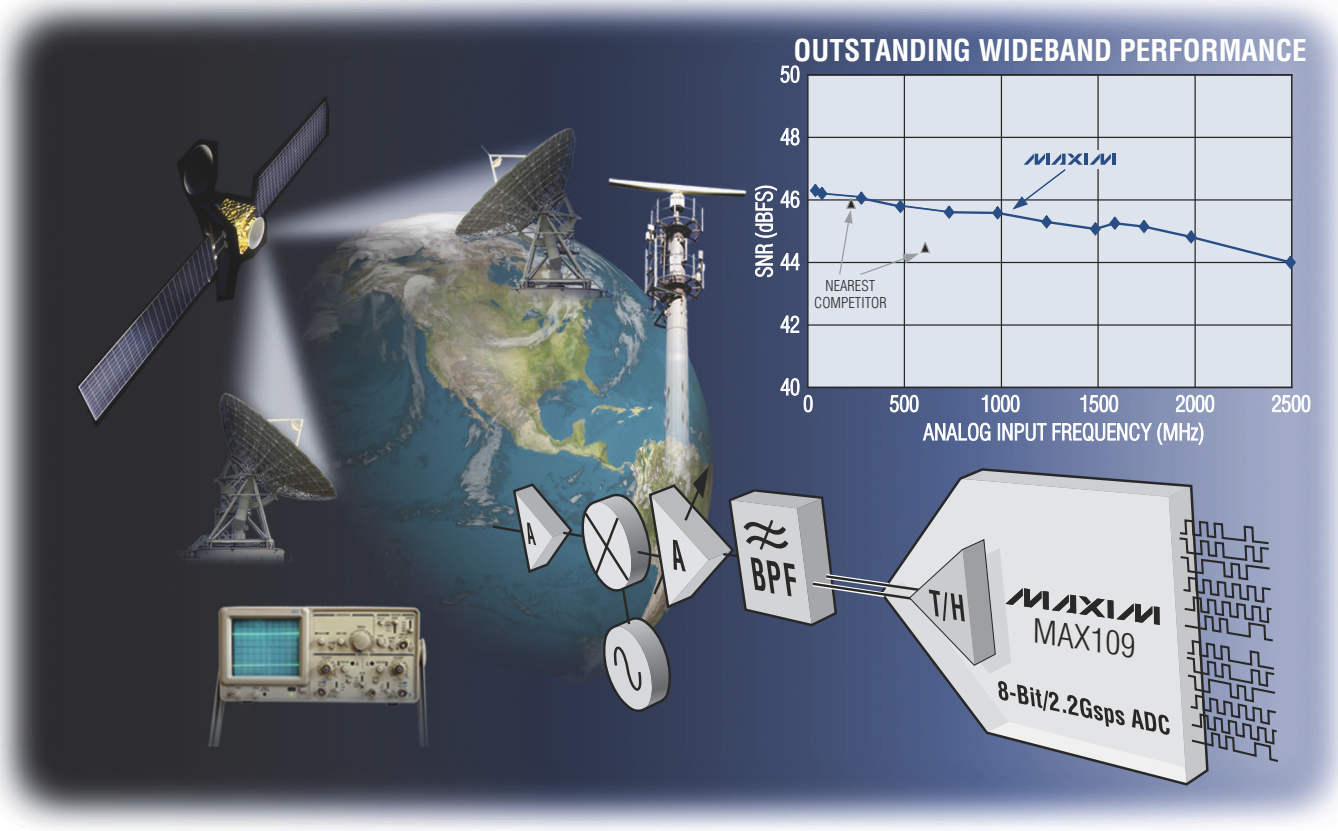
Kartik Joshi, Netaji Subhas Institute of Technology, New Delhi, India

Human interfaces for electronic gadgets sometimes require three states for control. A single-axis joystick has states to define motions to the right, to the left, and with no motion. Similarly, a timer has control buttons that allow the timer to increment, decrement, and remain untouched. Engineers usually create these interfaces by using two independent pushbuttons, requiring two microcontroller pins. This Design Idea presents a way to sense three states of an SPDT (single-pole/double-throw) switch with a center-off state, using only a single pin of

**TABLE 1 STATUS OF THE PIN FOR VALUES OF THE PORT AND THE DDR REGISTERS**

| | DDR bit=0<br>Port bit=0 | DDR bit=0<br>Port bit=1 |
|---|---|---|
| Pin connects to $V_{DD}$ through a resistor | Pin bit=1 | Pin bit=1 |
| Pin connects directly to ground | Pin bit=0 | Pin bit=0 |
| Pin connects to ground through a very-high-resistance path | Pin bit=0 | Pin bit=1 |

# 2.2Gsps, 8-BIT ADC ENABLES RF SAMPLING BEYOND NYQUIST

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- ♦ On-Chip 1:4 LVDS Demultiplexer
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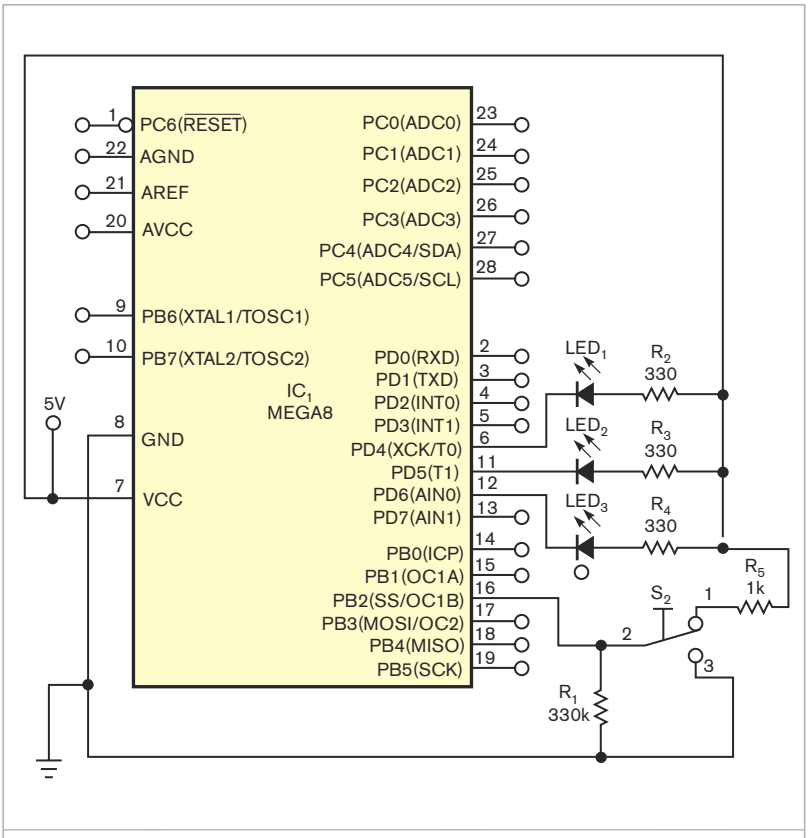


Figure 1 Using only one I/O pin, this circuit and a simple program can sense the state of a three-position switch.

Atmel's (www.atmel.com) ATmega8 microcontroller (**Reference 1** and **Figure 1**). **Listing 1**, which is available at the Web version of this Design Idea at www.edn.com/080221di1, is a simple program for the circuit.

The status of the pin of the microcontroller depends upon values of the DDR bit, the port bit, and its external connection. The microcontroller's pin connects to ground using pulldown resistor $R_1$ with resistance, typically, of a few hundred kilohms to impress the high-impedance state on the pin. You set the DDR register to zero. When the user toggles the switch to Position 1, the pin connects to $V_{DD}$ through resistor $R_5$, and the pin bit is one, regardless of the value of the port bit. When the user toggles the switch to Position 3, the pin is grounded, and the pin bit is zero, regardless of the value of the port bit. In the center-off state, the pin bit follows the port bit. **Table 1** summarizes the states of the pin for different values of the port and the external input. EDN

## REFERENCE

1 "ATmega8/ATmega8L 8-bit AVR with 8K Bytes In-System Programmable Flash," Atmel Corp, 2007, www.atmel.com/dyn/resources/prod_documents/2486S.pdf.

# AC-continuity tester finds single-ended faults in cables

Kevin Bilke, Maxim Integrated Products, Fleet, Hants, UK

An ac-based continuity tester for front-line test-and-repair jobs provides a simple go/no-go test for localizing faults in multiconductor cables (**Figure 1**). Open circuits are more likely to occur at the connector ends. This tool helps to identify the faulty end, thereby avoiding the risk of damaging a good connector by opening it. It's also useful for testing an installed cable for which both ends are in different locations. The circuit injects an ac signal on one wire of a cable and then looks for an absence of capacitive coupling to the other wires. After locating this fault, the circuit identifies the open wire and allows you to open and repair the correct cable end.

One end of a bad cable typically shows good ac continuity, and the other end typically has one or more connector pins with no ac continuity. Because a short in the cable appears as a good connection, the operator can easily confirm that the tester is operating correctly by simply shorting its test leads together. The first section of $IC_1$, a Maxim (www.maxim-ic.com) MAX9022 low-power dual comparator, forms a relaxation oscillator operating at approximately 155 kHz. It produces a peak-to-peak output signal approximately equal to the supply voltage, which feeds to a connector of the cable under test. The second section of the circuit processes any ac signal that the interlead capacitance picks up. A pair of silicon diodes first rectifies that signal and then integrates the rectified signal on storage capacitor $C_5$. Bleed resistor $R_5$ provides some noise immunity and helps to reset the capacitor between tests.

Output resistor $R_4$ and input capacitor $C_4$ provide limited circuit protection. The circuit indicates open for any test-cable capacitance below 100

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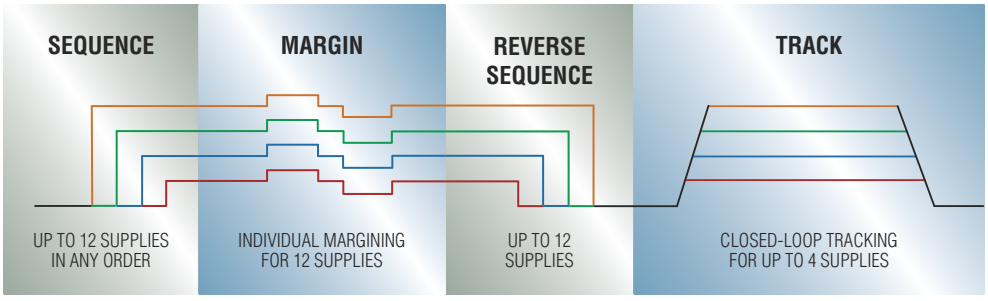
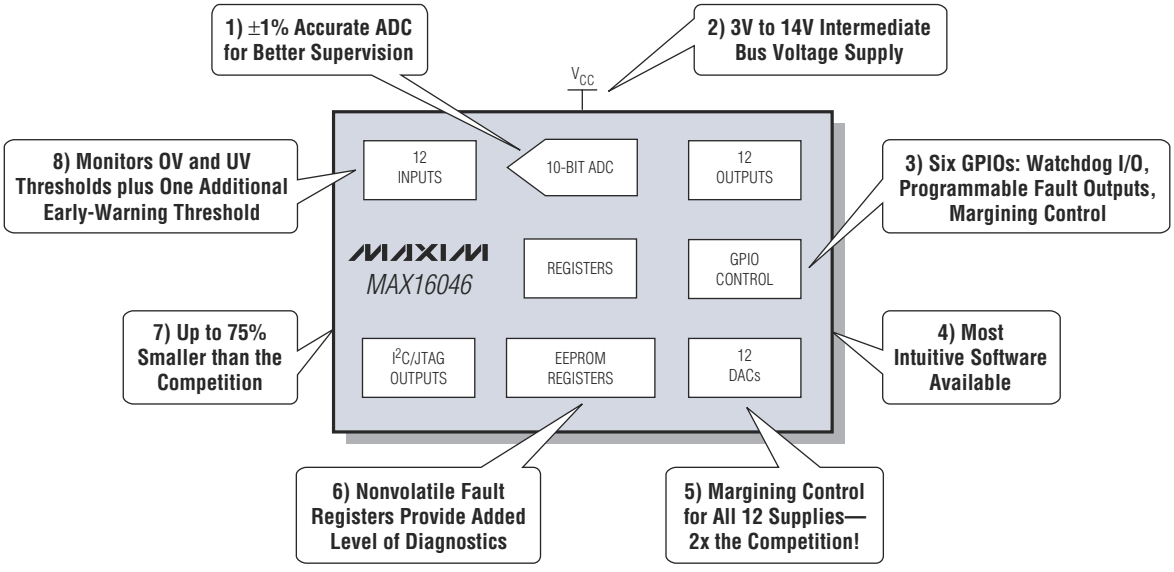



## EIGHT ADVANTAGES OVER THE COMPETITION




| Part | No. of Voltages Monitored | No. of Outputs/FET Drivers | Reverse Sequencing | Supply Adjustment/ Margining | ADC for Voltage Readback | No. of Voltages Tracked | Overvoltage Monitoring | Operates Off of Intermediate Bus Voltage | No. of GPIOs | Package (mm x mm) |
|---|---|---|---|---|---|---|---|---|---|---|
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| MAX16047 | 12 | 12/6 | | — | | | | | | |
| MAX16048* | 8 | 8/6 | | 8 DACs | | | | | | |
| MAX16049* | 8 | 8/6 | | — | | | | | | |

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pF. Thus, a standard mains-test lead, whose typical lead-to-lead capacitance is 200 pF, would test OK. The circuit is also immune to false triggering that the 60-Hz pickup from the power lines causes. Because the typical current draw of this low-power circuit is less than 40 µA, the circuit can usually operate from battery power in the form of three 1.5V AA or AAA cells. Many low-cost alternatives are available for the output device—for example, you could use a dc-activated piezoelectric buzzer—and most feature a suitably wide range of operating voltages. The 100-nF capacitors are standard ceramic decoupling capacitors, and the circuit contains no critical passive components. The comparator's high-side drive is somewhat better than its low-side drive, so it should source rather than sink current to the indicator device. $D_1$, $D_2$, and $D_3$ are silicon diodes. EDN

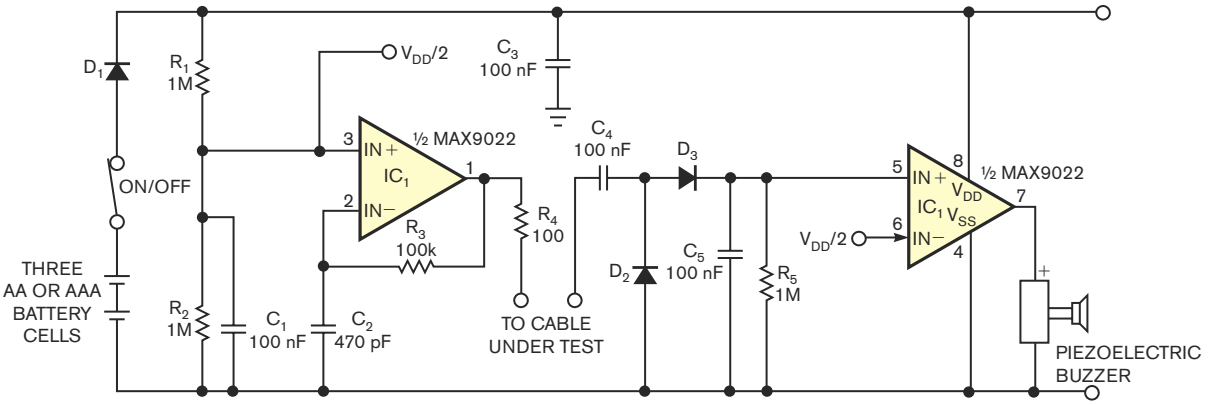
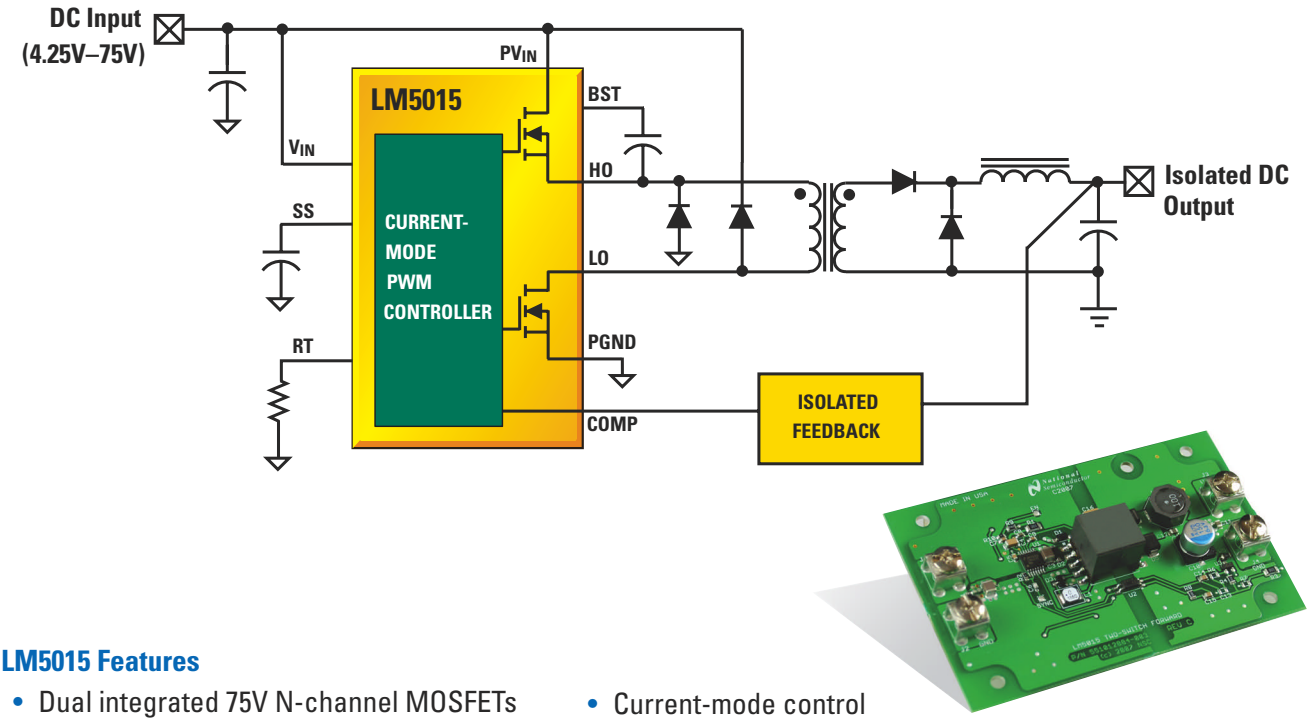



Figure 1 Based on a low-power dual comparator, this ac-continuity tester locates open-circuit pins in a cable.

# Industry's First High-Voltage Monolithic Two-Switch Forward DC-DC Regulator

national.com/power

## LM5015 Switch-Mode Regulator Features Ultra-Wide Input Voltage Range from 4.25V to 75V




### LM5015 Features

- Dual integrated 75V N-channel MOSFETs
- Ultra-wide input voltage range: 4.25V to 75V
- Adjustable output voltage
- Integrated current sensing and limiting
- Current-mode control
- Oscillator synchronization capability
- Programmable soft-start

| Product ID | $V_{IN}$ min (V) | $V_{IN}$ max (V) | Integrated Switches | Switch Voltage Rating (V) | Current Limit (A) | Package |
|---|---|---|---|---|---|---|
| **LM5000** | 3.1 | 40 | Low-Side | 75 | 2 | TSSOP-16 / LLP-16 |
| **LM5001** | 3.1 | 75 | Low-Side | 75 | 1 | SO-8 / LLP-8 |
| **LM5002** | 3.1 | 75 | Low-Side | 75 | 0.5 | SO-8 / LLP-8 |
| **LM5015** | 4.25 | 75 | Low- and High-Side | 75 | 1 | TSSOP-14EP |

### Applications

Communications, computing, industrial, medical, video, and test and measurement

**For FREE samples, datasheets, and more, visit:**

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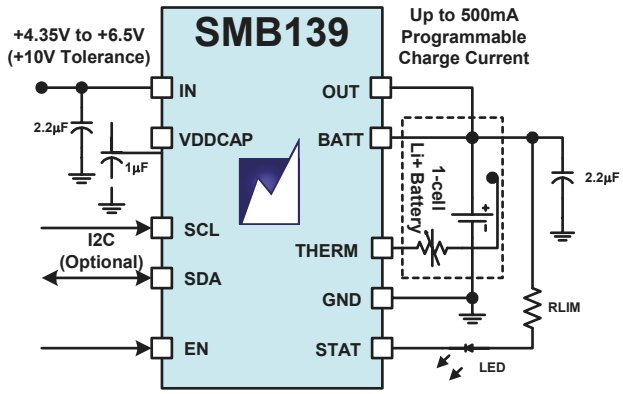
*The Sight & Sound of Information*

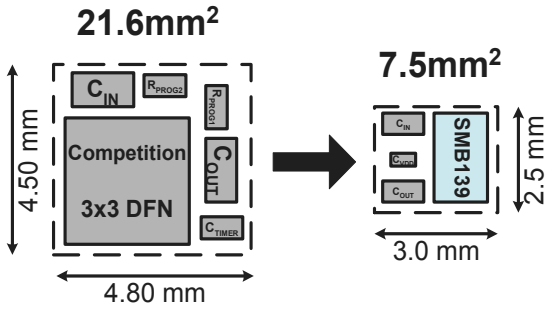
# World's Smallest Battery Charger!

## *SMB139 Packs Performance and Programmability in Tiny Package 500mA Charging Current - Ideal for Bluetooth™ Devices*




csr eXtension PARTNER

### *Shrink Solution Size by 65% vs. Existing Chargers*




## *SMB139 Applications*

- Bluetooth™ phone headsets
- Bluetooth™ stereo headphones
- Ultra-thin phones/media players
- Wristwatch GPS/MP3
- Sports/wearable electronics
- Portable biometric monitors

## *Summit's Programmable Battery Charger Family The Ideal Solution for Your Portable Application*

| | SMB137 | SMB138 | SMB135/235 | SMB139 |
|---|---|---|---|---|
| Topology | Switch-mode | Switch-mode | Switch-mode | Linear-mode |
| Input Voltage Range (V)* | 4.35 to 5.5 (16) | 4.35 to 6.0 (16) | 4.35 to 6.5 (10) | 4.35 to 6.5 (10) |
| # of Inputs/Outputs | 2/2 | 1/1 | 1/1 | 1/1 |
| Maximum Charge Current (mA) | 1500 | 1250 | 900 | 210/500 |
| TurboCharge™ Output | Automatic | Automatic | Software/uC | |
| CurrentPath™ Control | X | | | |
| USB On-The-Go Power | X | X | | |
| Low-Battery Recovery Mode | X | | | |
| I2C Interface | X | X | X | X |
| Programmable Float Voltage | X | X | X | X |
| Programmable Charge/Term. Current | X | X | X | X |
| Programmable Input Current Limit | X | X | | |
| Input/Battery OV/UV | X | X | X | X |
| Hardware Safety Timer | X | X | X | X |
| Software Watchdog Timer | X | X | | |
| Battery Thermal Protection | X | | X | X |
| IC Thermal Protection | X | X | X | X |
| Package | 3.6x3.3 CSP-30 | 3.1x2.1 CSP-20 | 2.1x1.3 CSP-15<br>5x5 QFN-32 | 2.1x1.3 CSP-15<br>5x5 QFN-32 |
| Solution Size (mm2) | 50 | 28 | 31 | 7.5 |

* () Indicates overvoltage "holdoff" tolerance

*For more information see:*

***www.summitmicro.com/SMB139***

SUMMIT MICROELECTRONICS

*Programmable Power for a Green Planet™*

# productroundup

## SWITCHES AND RELAYS

### Tactile switches allow complete sound-intensity control

The KSC ST sound-tunable tactile-switch series enables 100% control of sound intensity. The switches provide the ability to match the sound level of applications with two sound-intensity grades, ranging from 30 to 50 dBa. Aiming at automotive applications, such as steering wheels; heating, ventilation, and air conditioning; dashboards; and door, seat, and sunroof modules, the switch series also suits industrial-control panels and medical and consumer applications. The KSC ST switches cost 19 cents each (10,000).

**C&K Components, www.ck-components.com**

### Power-relay series switches 200A at 400V dc

The G9E dc-power-relay series provides a means of disconnection in high-power-battery applications. The relays feature a sealed, gas-filled construction for cooling the arc created during switching. Reducing the contact gap improves operating noise and allows a 70% reduction in overall size, compared with contactors. Operating-coil voltages include 12, 24, 48, 60, and 100V dc. The G9EA measures 36×73×67.2 mm in versions operating at 60A at 400V dc and 100A at 120V dc; the G9EC measures 44×98×86.7 mm in a version operating at 200A at 400V dc; and the G9EB measures 25×60×58 mm and switches 25A at 250V dc. The devices are available in an SPST-NO (single-pole/single-throw/normally open) contact configuration. The G9EA sells for $110 to $140, the G9EB sells for $99 to $103, and the G9EC sells for $220 to $240.

**Omron Electronic Components LLC, www.components.omron.com**

### SPDT analog switches have low on-resistance

The DG469 and DG470 high-voltage, single- and dual-supply SPDT (single-pole/double-throw) analog switches provide 3.6Ω on-resistance and 0.4Ω flatness. The switches provide an enable pin for maintaining a safe state at power-up and prevent accidental signal or power shorts, and the DG470's enable pin puts all of the switches in a

# *EDN's 18th Annual* INNOVATION AWARDS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# productroundup

## SWITCHES AND RELAYS

high-impedance state. The switches offer a typical 3.6Ω and a maximum 4.2Ω on-resistance with 0.4Ω flatness. Providing 120-mA continuous current and suiting relay replacement and power routing, the devices provide a 44V maximum supply-voltage rating and 57-dB isolation at 1 MHz. Available in −40 to +85 and −40 to +125°C temperature ranges, the DG469 and DG470 analog switches cost 70 cents each (1000).

**Vishay Intertechnology, www.vishay.com**

### Switch series integrates two slew-rate-controlled load switches

Combining two low-resistance, slew-rate-controlled load switches, the AAT4282A load switch provides two MOSFETs with 60-mΩ typical on-resistances at 5V. Suiting high-side, load-switching applications, the device supports 3 and 5V systems by operating over a 1.5 to 6.5V input range. Features include a 1-µA quiescent current and 2.5 to 5V CMOS- and TTL-compatible input-logic levels. The AAT4282A-1 targets slew-rate-limited load switches; the AAT4282A-2 provides turn-on capabilities for applications requiring less-than-500-nsec systems and typical turn-off speeds of less than 3 µsec; and the AAT4282A-3 has a minimized slew-rate-limited turn-on function and a shutdown-output-discharge circuit to turn off a load when the switch is disabled. Available in a 2×2-mm FTD-FN22-8 package, the AAT4282A costs $1.07 (1000).

**Advanced Analogic Technologies, www.analogictech.com**

## EDN ADVERTISER INDEX



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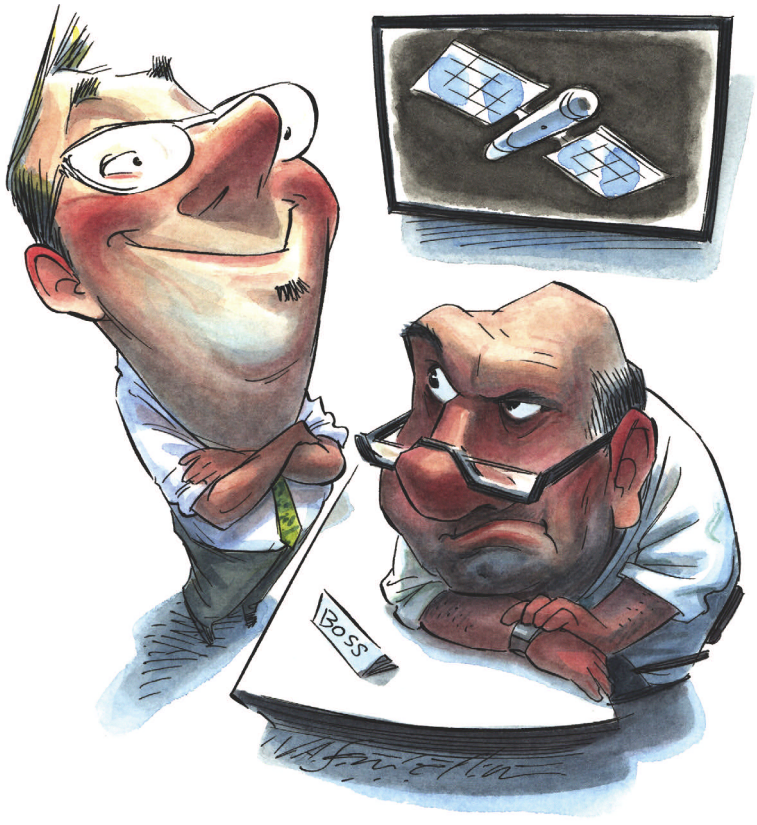
BY STEVE LUBS • DEPARTMENT OF DEFENSE

# A helping hand




DANIEL VASCONCELLOS

Early in my career, I designed several kinds of signal demodulators, including AM, FM, and PM devices. Two of our standard building blocks were analog multipliers and discrete integrators. My boss was moving, albeit slowly, from analog to digital techniques, so he and I looked at simple ways to make a digital equivalent of these two blocks.

After four months' effort on what we thought was a simple design, my boss called it quits. I used most of the parts from our attempts in other projects and threw away the rest—except for a pair of MAC (multiplier-accumulator) ICs.

In those days, we designed with 74XXX and 74LSXXX MSI counters, registers, and gates. The MACs were TTL (transitor-to-transistor logic), 8×8-bit-multiply, 64-bit-output devices, specially ordered for this application. In power consumption, they made the 74XXX stuff look like CMOS, so my boss didn't see where we'd use them in any other projects. I kept them, however, thinking of various ways they might be useful. One day, while looking at their data sheet, I realized one would make a fast 64-bit up/down counter.

**I DIDN'T RECEIVE ANY AWARDS OR PATS ON THE BACK, BUT MY IDEA DID HELP ANOTHER ENGINEER.**

I presented the idea to my boss. His first reaction was to stare at me. Then he warned, "It's too big. It uses too much power. It's too expensive." Finally, he asked, "Don't you have something useful to do?"

Intimidated, but not defeated, I further developed my idea and ran a few tests. The design worked beautifully. However, when I showed it to my co-workers, reactions varied from loud yawns to inquiries of "Is that *all* it does?" Lacking other encouragement, I submitted it to *EDN* as a Design Idea. The magazine accepted it.

I didn't receive any congratulations from management, but I didn't mind. After all, a professional magazine had published my idea—an achievement that made me proud … for the next three months. It was then that I read a letter to the editor in *EDN*, ranting about the Defense Department's wasting of taxpayer money and pointing to my design as a prime example. I sat down and began writing a rebuttal but realized I would be better off showing how my idea would be an improvement. I tried to use it in other projects, but my boss always had a "better" suggestion. (Well, he *was* my boss.)

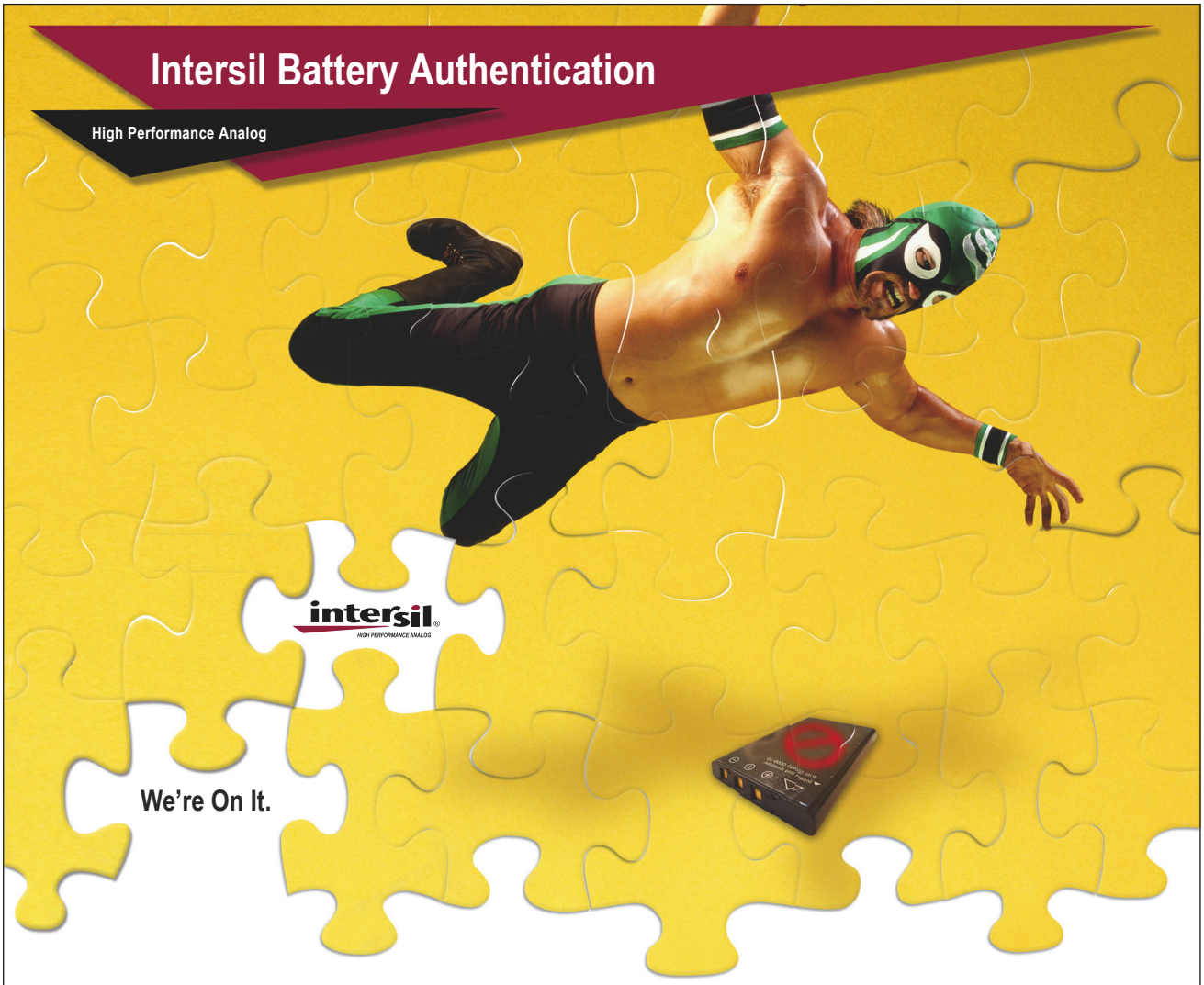
I put the matter aside and forgot about it. Then, almost a year later, I received a call from an engineer who had questions about the circuit's operation. He needed a 64-bit counter for a box he was designing for a NASA (National Aeronautics and Space Administration) satellite. My idea not only saved board space, using one 100-pin IC rather than 16 16-pin ICs plus wiring, but also simplified the board layout, which meant easier testing and lower cost.

I didn't receive any awards or pats on the back, but my idea did help another engineer; that kind of satisfaction goes a long way. I'd like to believe that my other published Design Ideas have helped others, just as those I've read have helped me—especially when six cups of black coffee lose their effect on the meetings and paperwork, and I need something new to perk me up. EDN

***Steve Lubs has been an engineer in a variety of roles at the Defense Department for 30 years and has always argued with his bosses. Like Steve, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.***

# Intersil Battery Authentication

High Performance Analog

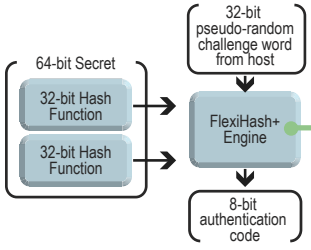



## Intersil's **ISL9206 FlexiHash+™ Engine delivers high-security battery authentication** at a low cost.

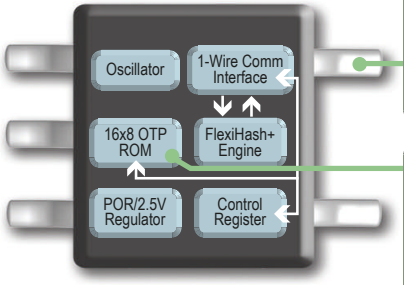
Intersil's ISL9206 is an easy-to-use, robust, and inexpensive battery authentication solution for 1-cell Li-Ion/Li-Polymer or 3-cell NiMH series battery packs.

**ISL9206 Key Features:**

- Challenge/response-based authentication scheme using 32-bit challenge code and 8-bit authentication code.
- FlexiHash+ engine uses two sets of 32-bit secrets for authentication code generation.
- 16x8 one-time programmable ROM memory.
- Additional programmable memory for storage.




Patent pending FlexiHash+ engine consists of four separate programmable CRC calculators. Two sets of 32-bit secret codes are used for authentication code generation.




XSD single-wire host bus interface communicates with all 8250-compatible UARTs or a single GPIO pin. Supports CRC on read data and transfer bit-rate up to 23Kbps.

16 bytes of one-time programmable ROM memory for storage of pack information and ID, device authentication secrets, device default settings, and factory-programmed trim parameters.

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